PAGE3;RESERVE RN65~71 P/L 49.9ohms for ICS951464
PAGE3;CHANGE R107,R108 from 47.5 ohms TO 0ohm;Need CHECK!!
PAGE14;CHANGE LCD1;PIN27 TO IP105;RESERVE FOR LIGHT SENSOR
PAGE14;CHANGE LCD1;PIN24 TO 5V POWER RAIL FOR LED DRIVER BOARD IC ENABLE PIN(HIGH ACTIVE)
PAGE14;CHANGE F1 TO 4A
PAGE14;P/U TMDS DDC DAT TO 3D3V S0,ADD R471
PAGE15;CHANGE R184,R185,R188 FROM 75ohms TO 150 ohms
PAGE19;SWAP USB PAIR OF FT AND MINICARD

PAGE27;CHANGE Q11 TO 84.00143.B1K
PAGE30;CHANGE C389,C390 TO 1uF,X5R
PAGE30;CHANGE R450,R453 TO 14Kohms
PAGE30;CHANGE R459,R463 TO 40.2ohms
PAGE30;CHANGE R458,R462 TO 33ohms
PAGE31;ADD R472 AND P/H TO 3D3V S0 FOR CAPA_INT#
PAGE31;CHANGE R347 TO 4.7Kohms(E51_TxD P/L)
PAGE31
1.KBC Beep change from A_PWM0(32) to GPIO56(31)
2.Power LED change from GPIO32(65) to A_PWM0(32)
3.e-Button LED change from GPIO43(20) to A_PWM1(118)

LAYOUT

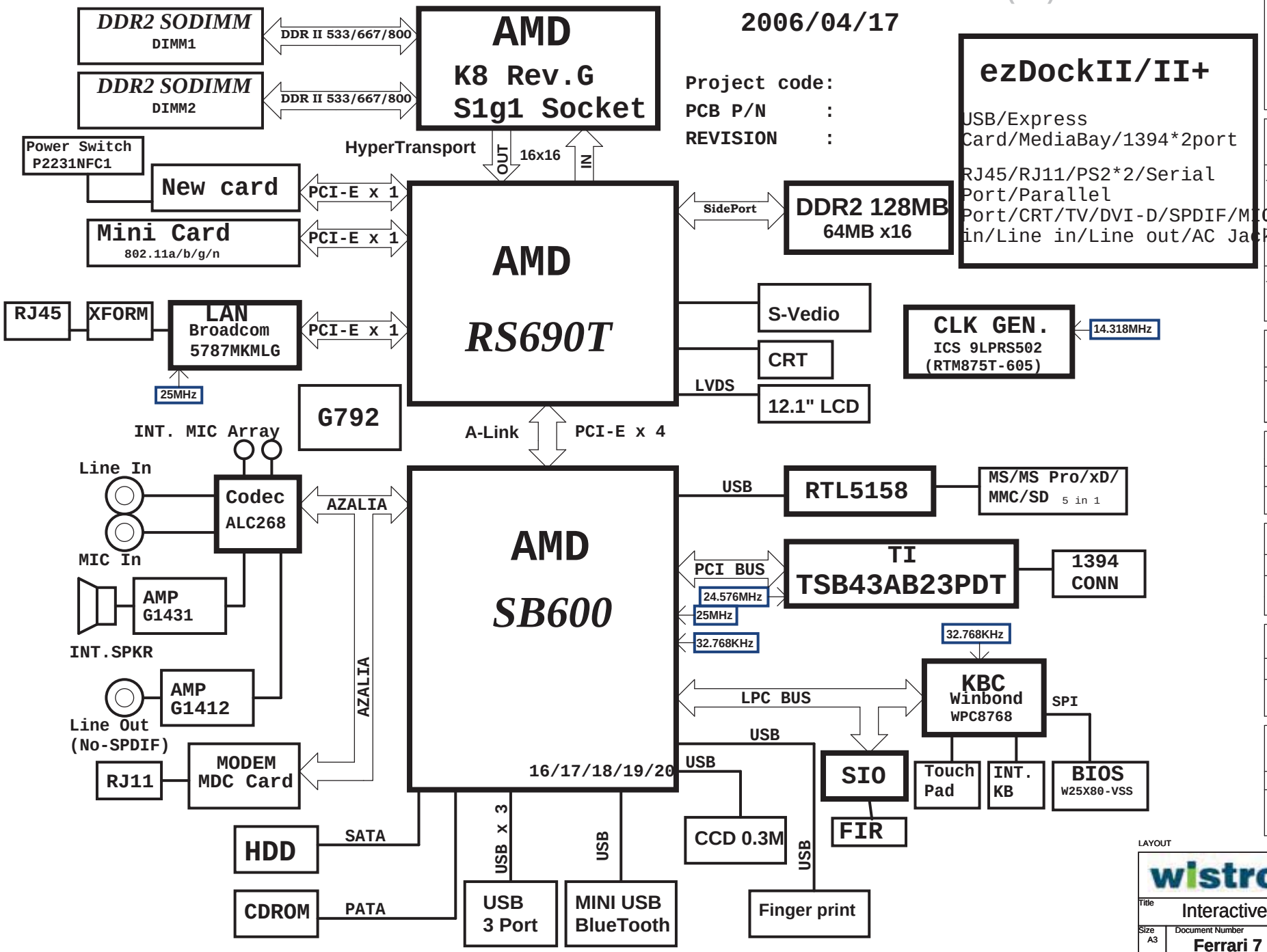
wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	Change List
Size A	Document Number: Ferrari 7 — Rev SA
Date: Thursday, August 02, 2007	Sheet 1 of 47

Ferrari 7 Block Diagram

Ver: Friday Practice (SA)
Saturday Practice (SB)
Qualifying(SC)
Race(-1)

2006/04/17

Project code:
PCB P/N :
REVISION :



PCB Layer Stackup

- L1: Component
- L2: GND
- L3: Signal
- L4: VCC
- L5: Signal
- L6: Signal
- L7: GND
- L8: Component

CPU V_CORE ISL6264 38/39

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC TPS51124 47

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC ISL6236 46

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO TPS51100 48

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO APL5915 48

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO ISL6236 46

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger ISL6255 42

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

LAYOUT

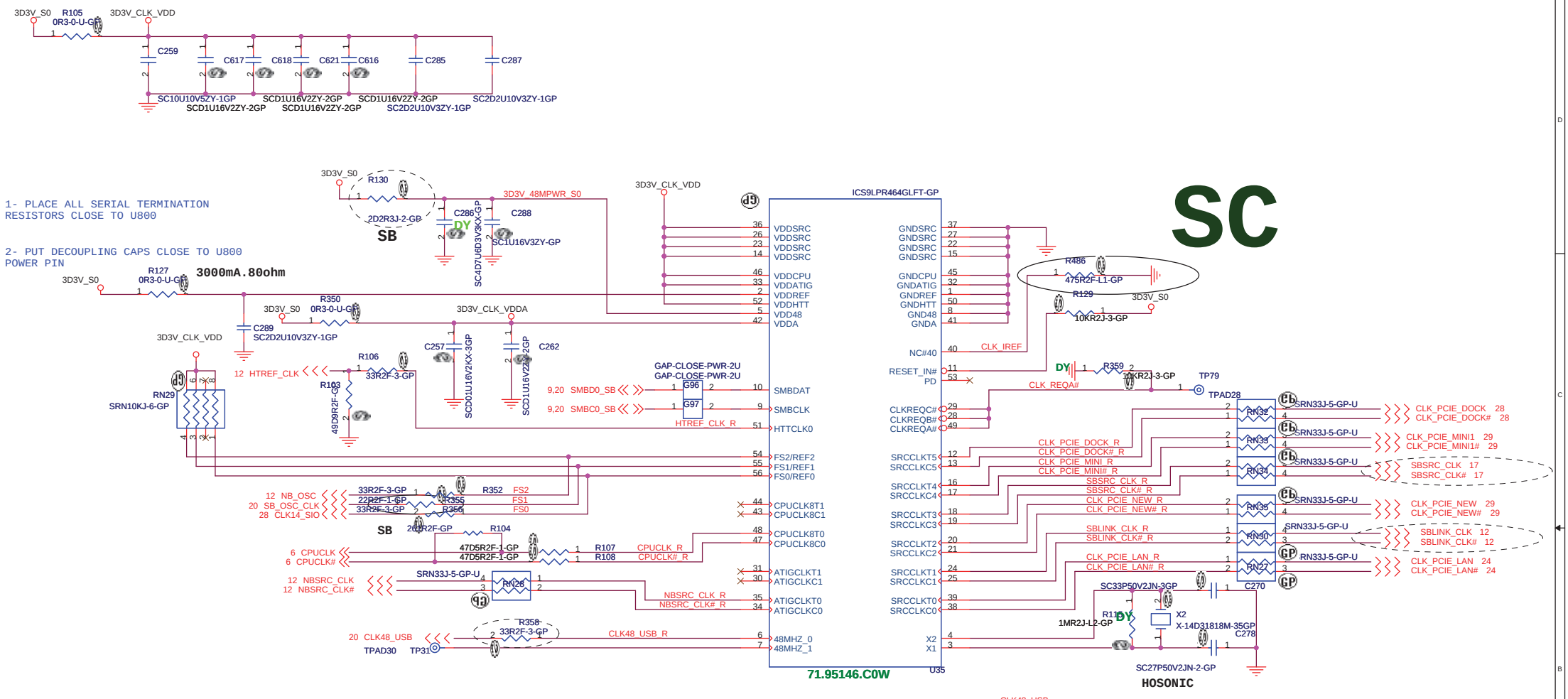
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Interactive Circuit Map

Size: A3 | Document Number: Ferrari 7 | Rev: SA

Date: Thursday, August 02, 2007 | Sheet 2 of 47



Check SLGO EXT CLK XSL84606 (56 Pin) or XSL84605 (64 Pin) pin to pin compatable with ICS951464

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

LAYOUT

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: *CLKGEN_ICS951464*

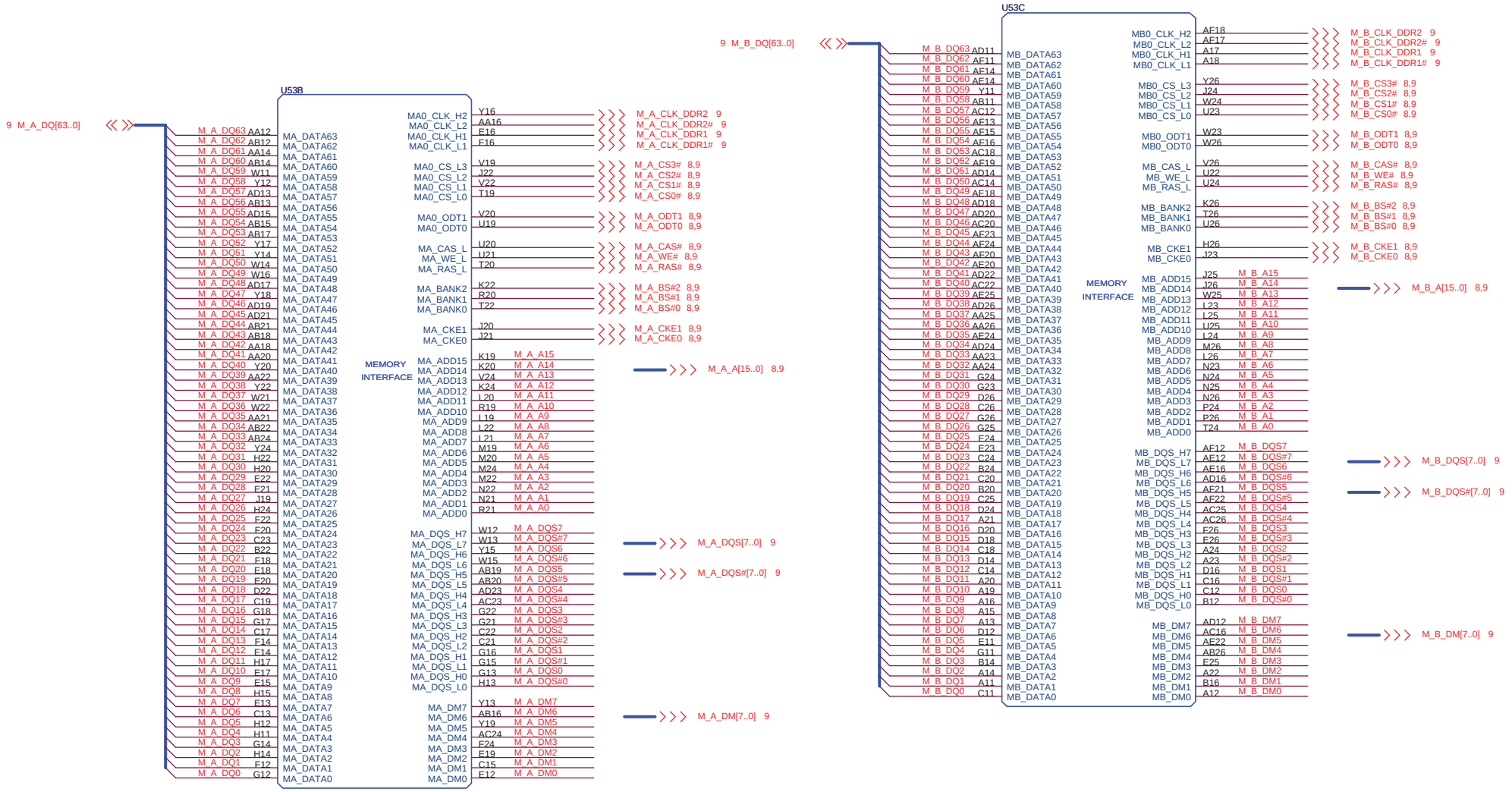
Size: A3 | Document Number: Ferrari 7 | Rev: SB

Date: Thursday, August 02, 2007 | Sheet 3 of 47

62.10055.111

LAYOUT

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU(1/4)_HyperTransport I/F***	
Size A3	Document Number **Ferrari 7**	Rev SB
Date: Thursday, August 02, 2007	Sheet 4 of 47	



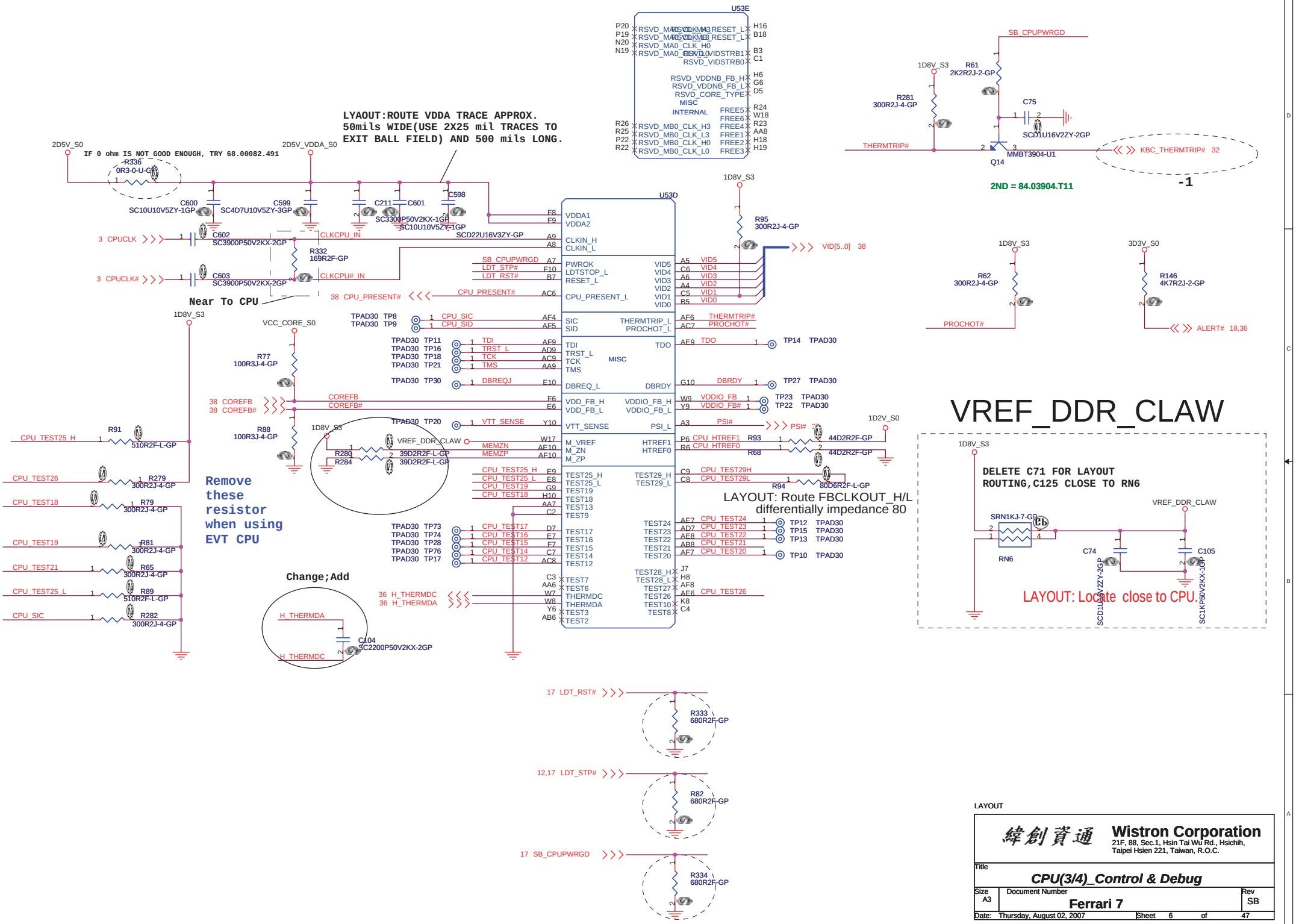
LAYOUT

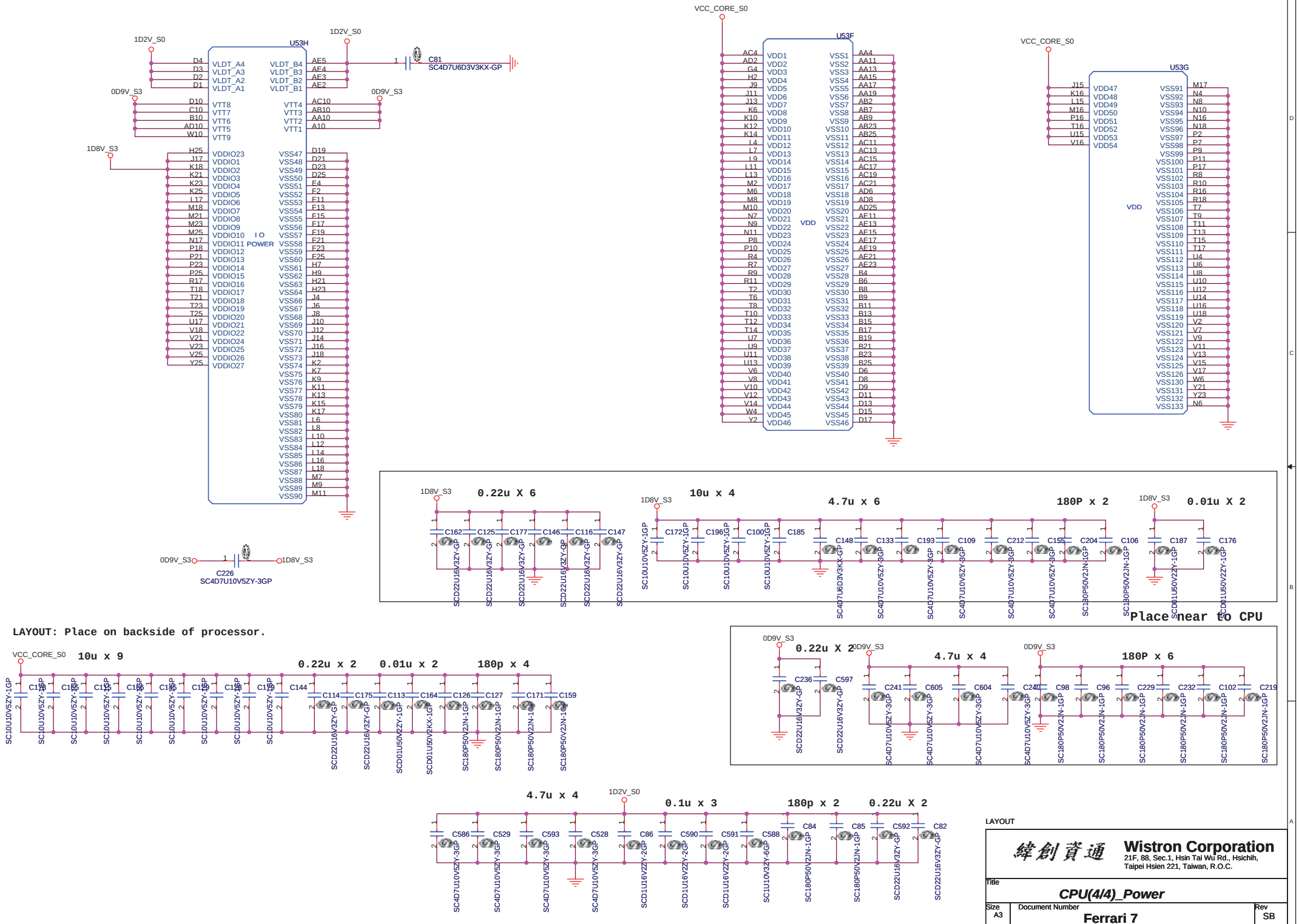
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU(2/4)_DDR***

Size	Document Number	Rev
A3	**Ferrari 7**	SB

Date: Thursday, August 02, 2007 Sheet 5 of 47


LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.
IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491
Near To CPU
Remove these resistor when using EVT CPU
Change;Add
LAYOUT: Route FBCLKOUT_H/L differentially impedance 80
VREF_DDR_CLAW
DELETE C71 FOR LAYOUT ROUTING,C125 CLOSE TO RN6
LAYOUT: Locate close to CPU
2ND = 84.03904.T11
-1
U53E
U53D
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU(3/4)_Control & Debug
Size A3
Document Number
Ferrari 7
Rev SB
Date: Thursday, August 02, 2007
Sheet 6 of 47



LAYOUT

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

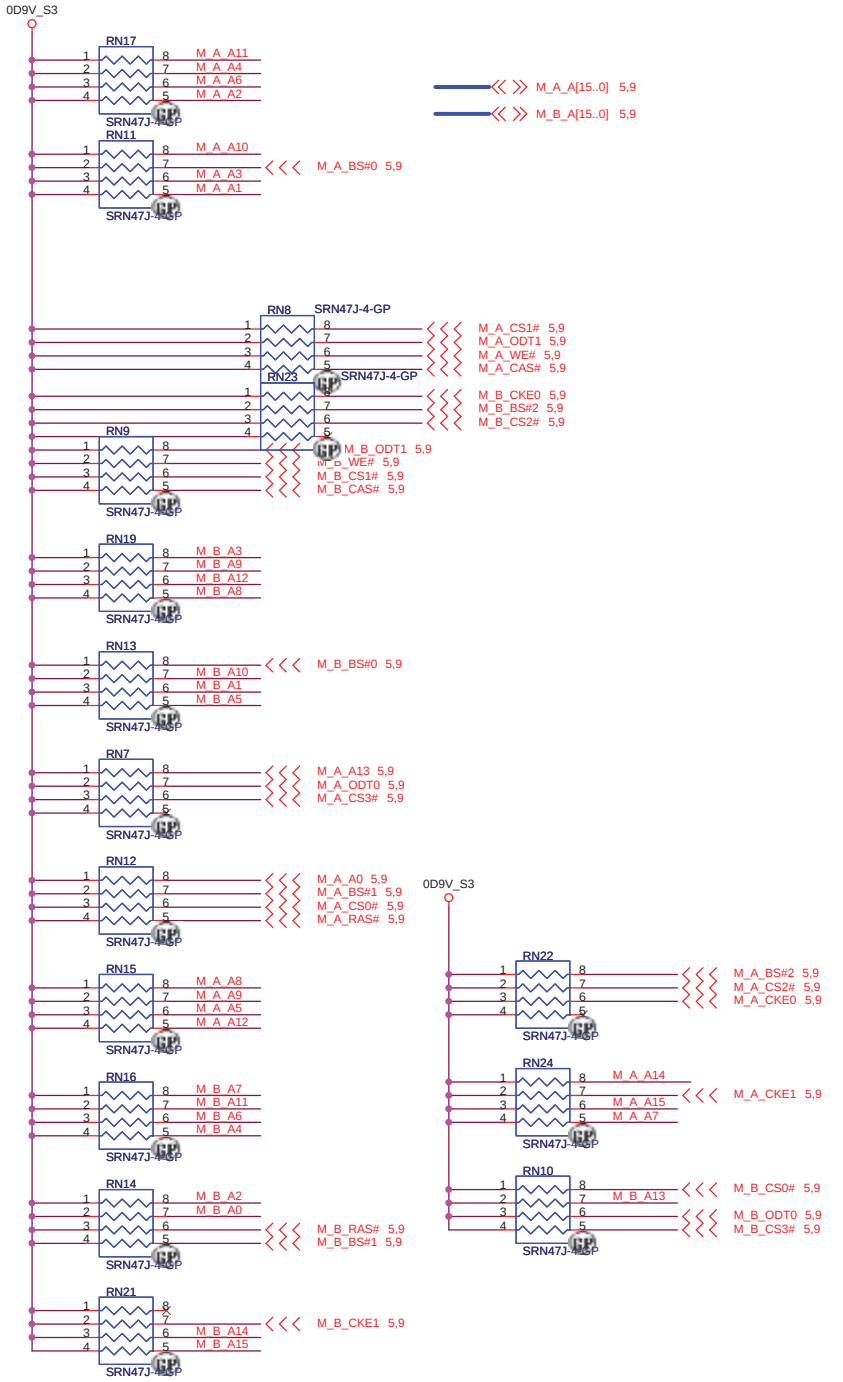
Title: CPU(4/4)_Power

Size: A3 | Document Number: Ferrari 7 | Rev: SB

Date: Thursday, August 02, 2007 | Sheet 7 of 47

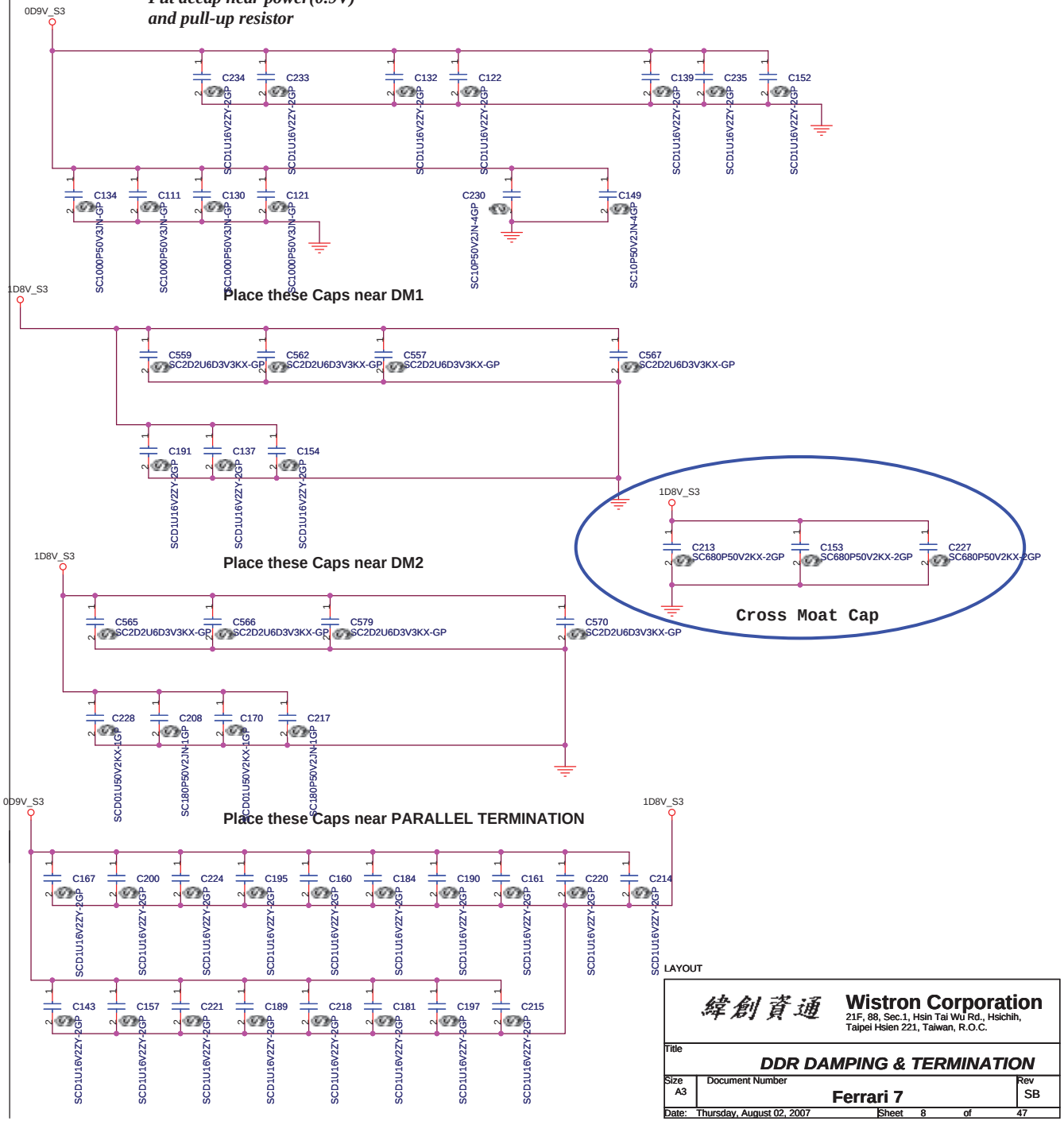
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor



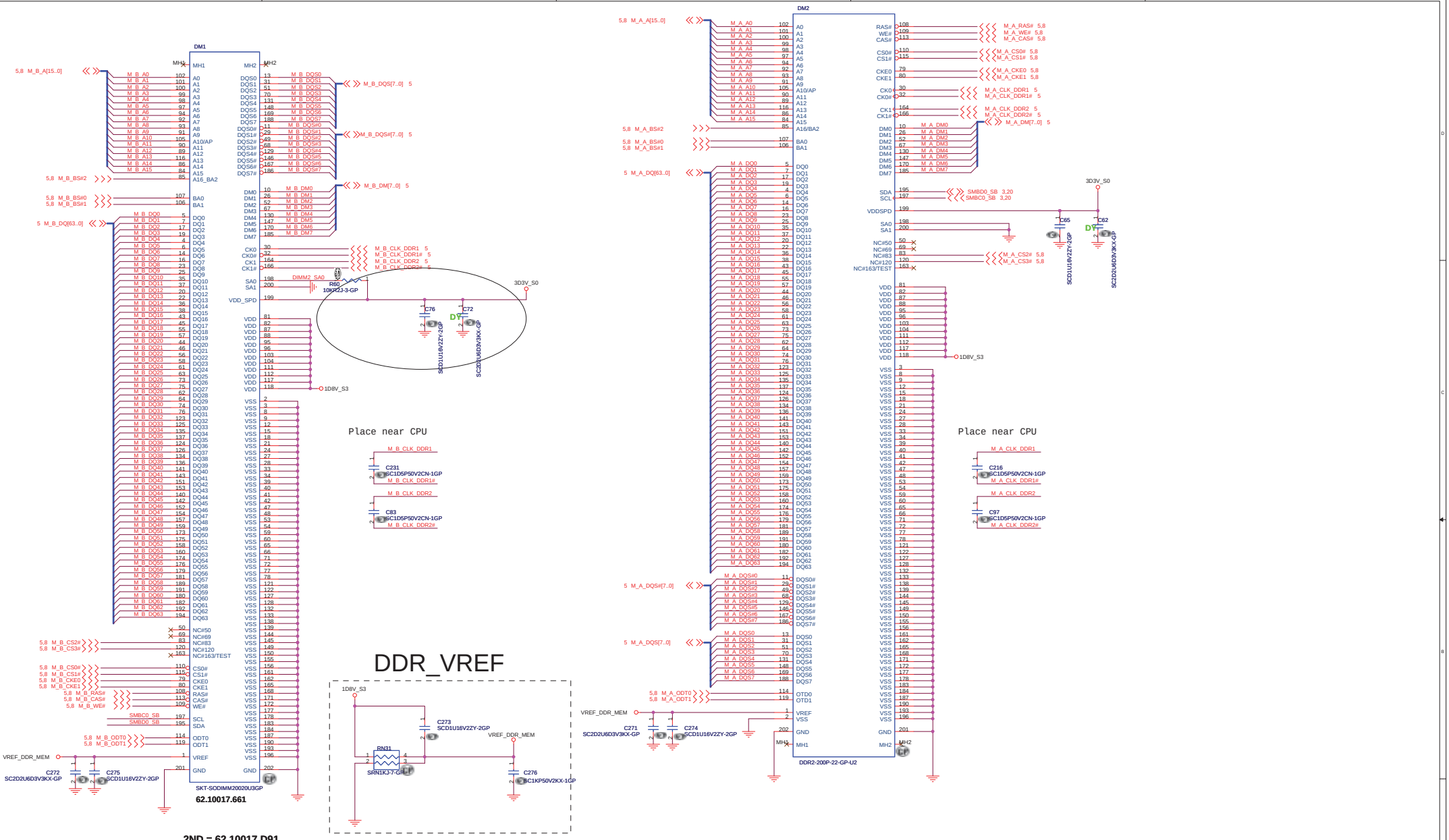
Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor



LAYOUT

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DDR DAMPING & TERMINATION***	
Size A3	Document Number **Ferrari 7**	Rev SB
Date: Thursday, August 02, 2007	Sheet 8 of 47	



LAYOUT

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

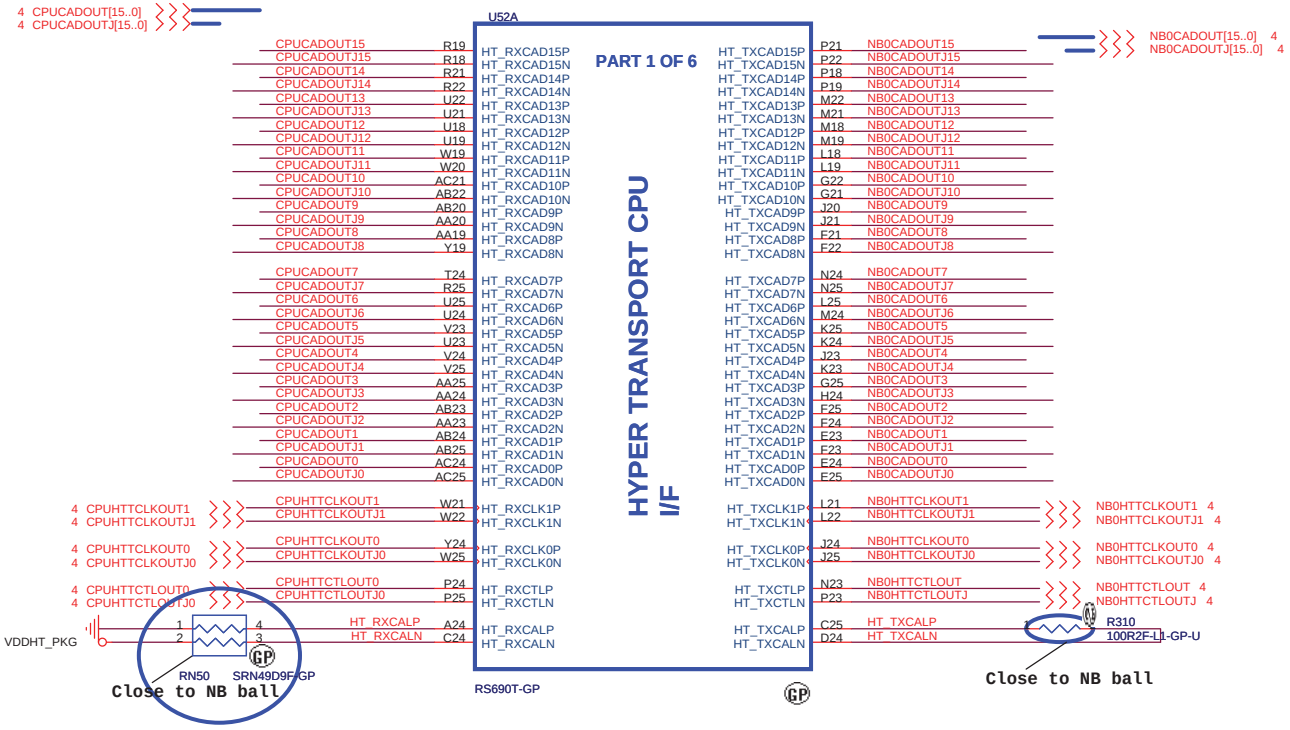
Title: ***DDR SO-DIMM SKT***

Size	Document Number	Rev
A2	Ferrari 7	SB

Date: Thursday, August 02, 2007 Sheet 9 of 47

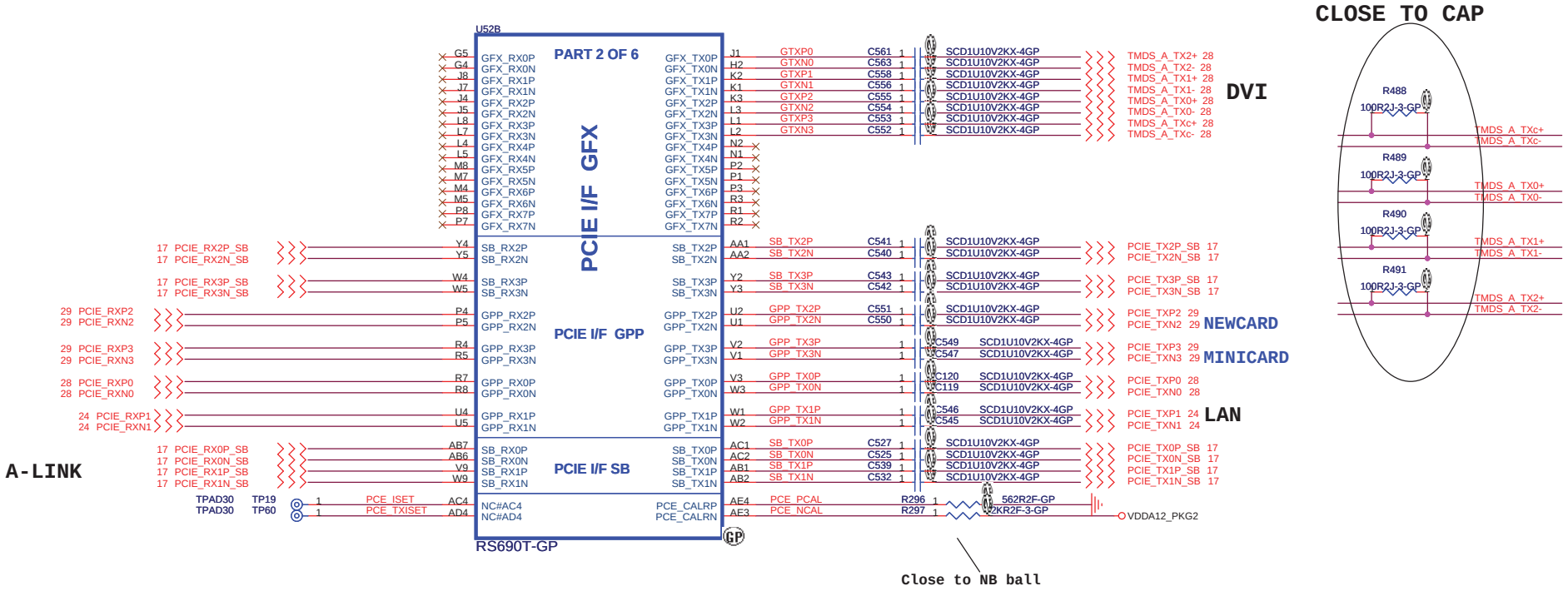
CLAW HAMMER TO NB

NB TO CLAW HAMMER



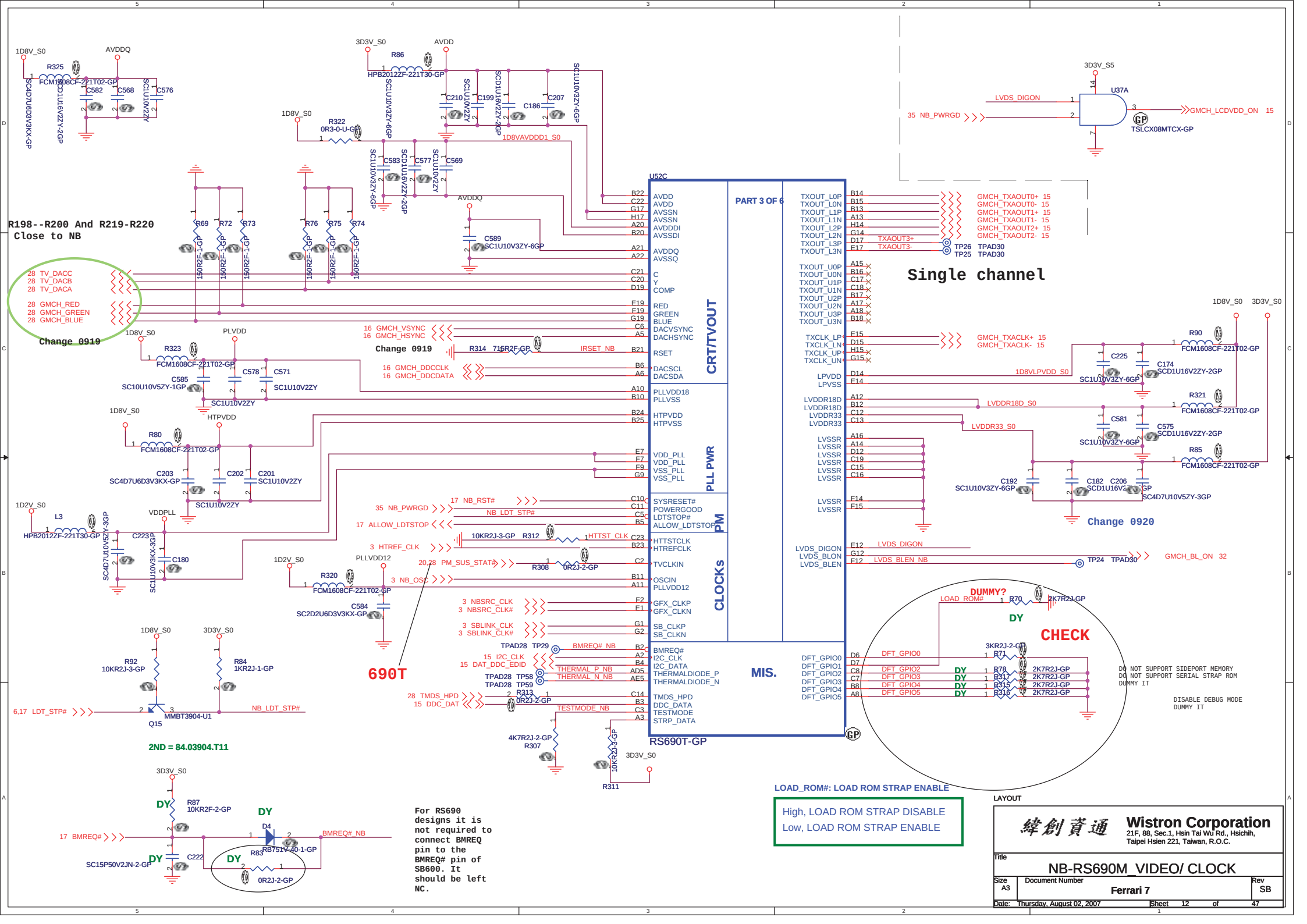
LAYOUT

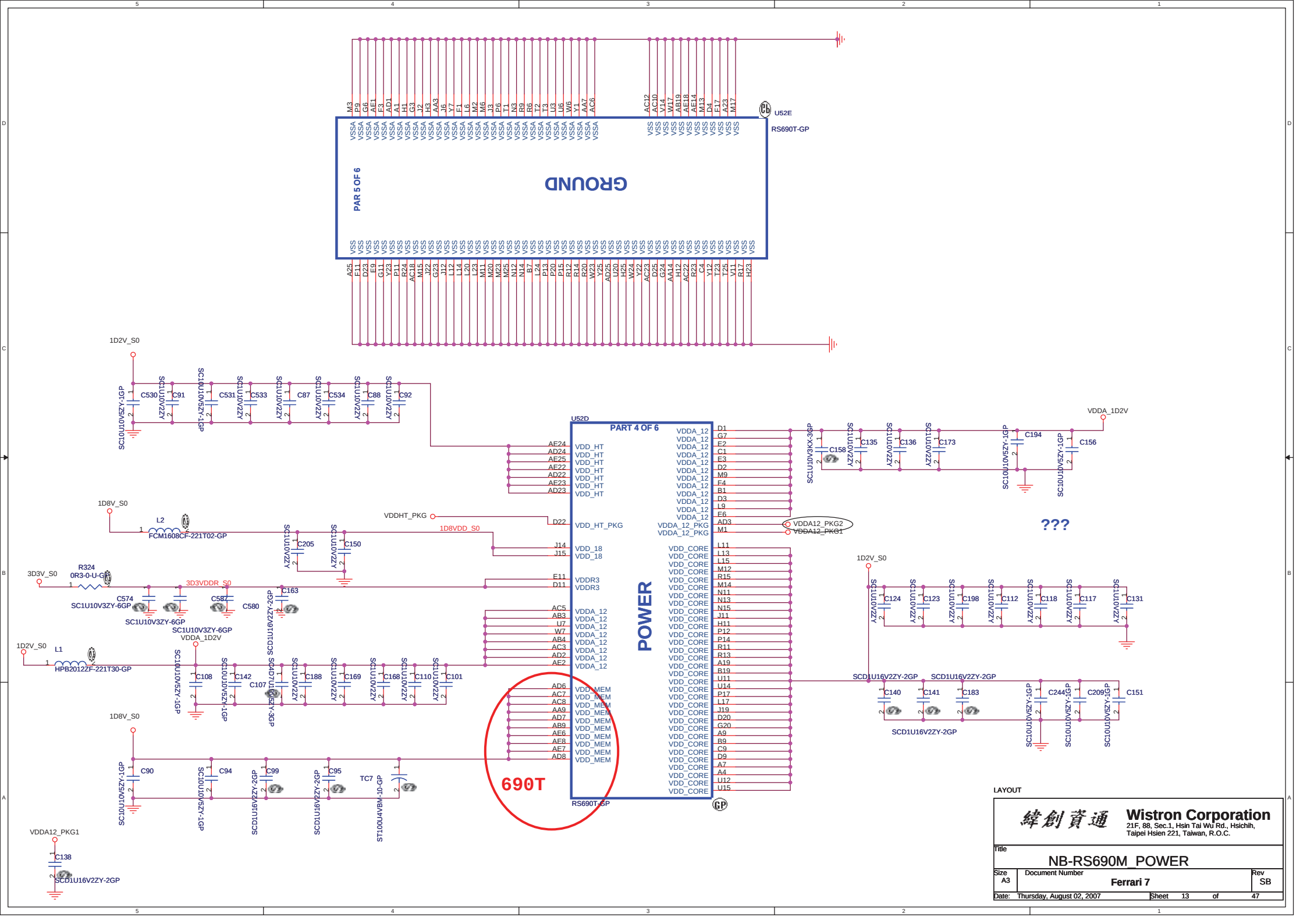
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***NB-RS690T_HT***
Size A3	Document Number **Ferrari 7** Rev SB
Date: Thursday, August 02, 2007	Sheet 10 of 47

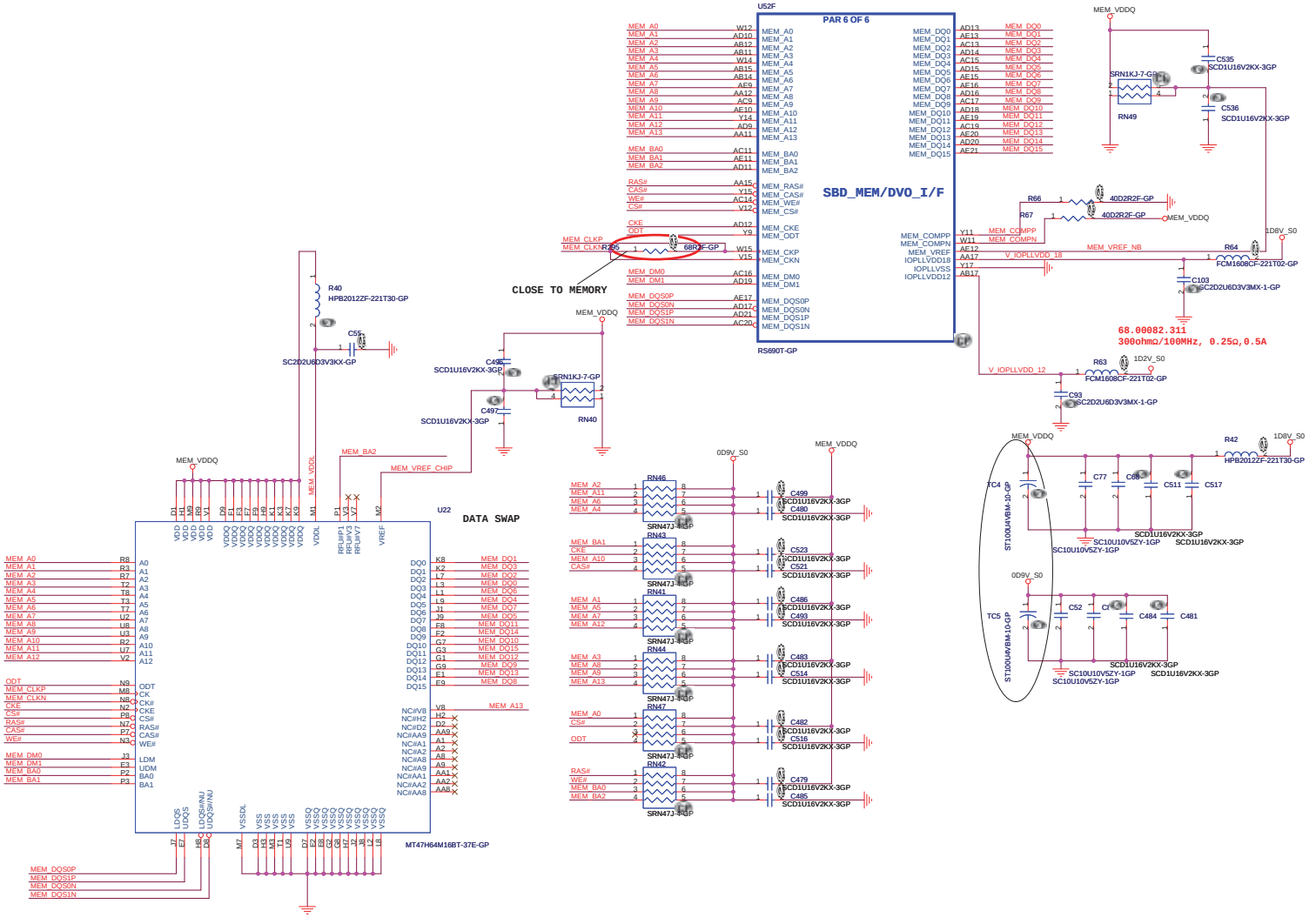


LAYOUT

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	NB-RS690M_MEM/PCIE_LINK I/F
Size A3	Document Number: Ferrari 7 — Rev SB
Date: Thursday, August 02, 2007	Sheet 11 of 47


R198--R200 And R219-R220
Close to NB
Change 0919
Change 0919
Single channel
Change 0920
690T
2ND = 84.03904.T11
U52C
RS690T-GP
PART 3 OF 6
CRT/TVOUT
PLL PWR
PM
CLOCKs
MIS.
U37A
TSLCX08MTCX-GP
DUMMY?
CHECK
DY
LOAD_ROM#: LOAD ROM STRAP ENABLE
High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE
For RS690 designs it is not required to connect BMREQ pin to the BMREQ# pin of SB600. It should be left NC.
DO NOT SUPPORT SIDEPORT MEMORY
DO NOT SUPPORT SERIAL STRAP ROM
DUMMY IT
DISABLE DEBUG MODE
DUMMY IT
LAYOUT
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
NB-RS690M_VIDEO/ CLOCK
Size A3
Document Number
Ferrari 7
Rev SB
Date: Thursday, August 02, 2007
Sheet 12 of 47


U52E
RS690T-GP
PAR 5 OF 6
GROUND
U52D
PART 4 OF 6
POWER
RS690T-GP
690T
1D2V_S0
1D8V_S0
3D3V_S0
VDDA_1D2V
VDDA12_PKG1
VDDHT_PKG
1D8VDD_S0
3D3VDDR_S0
VDDA12_PKG2
VDDA12_PKG1
???
LAYOUT
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
NB-RS690M_POWER
Size A3
Document Number
Ferrari 7
Rev SB
Date: Thursday, August 02, 2007
Sheet 13 of 47



2ND = HYNIX 32M*16 72.51216.F0U; 72.18512.M0U Qimonda 32M*16

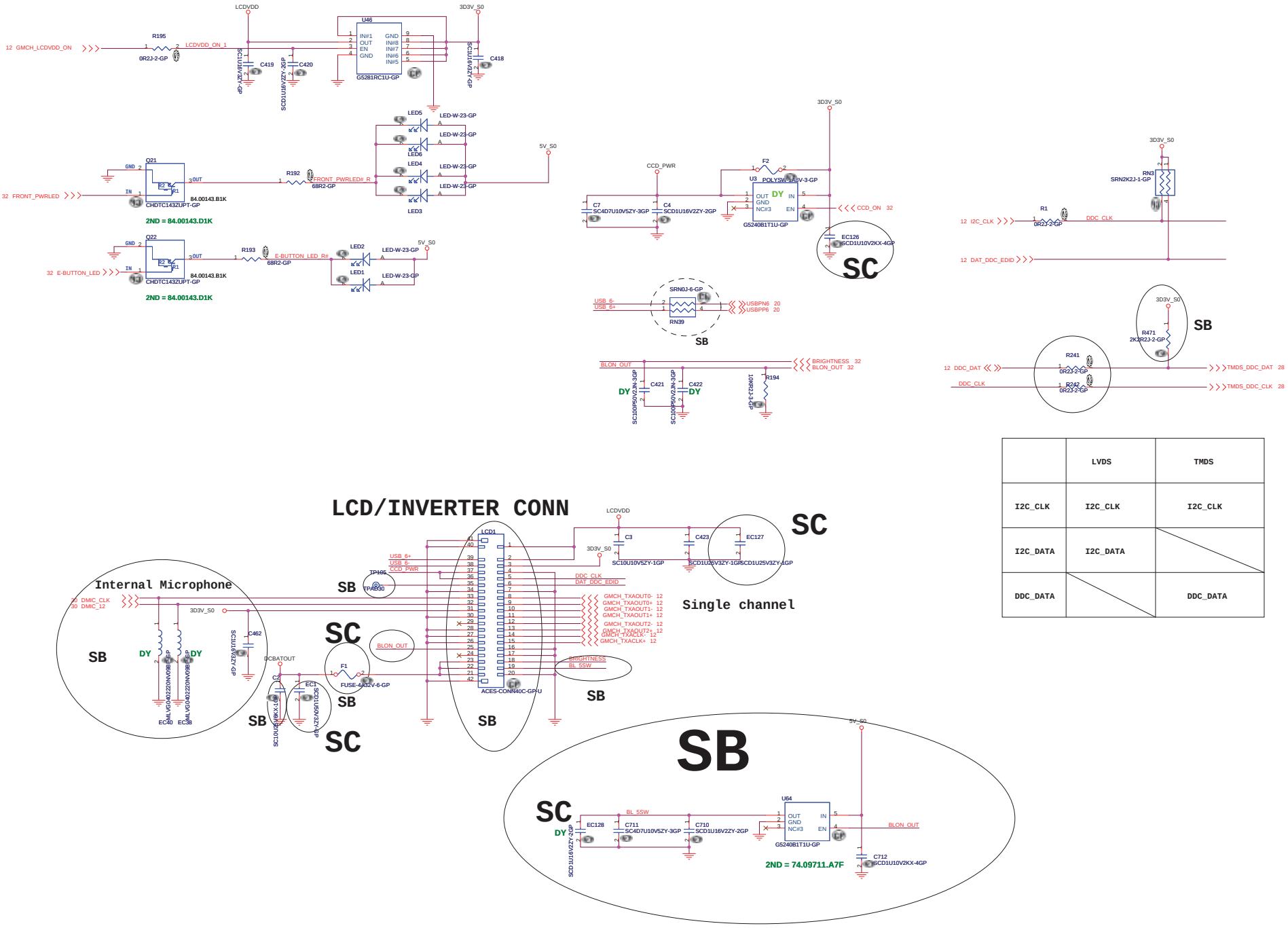
LAYOUT

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NB-RS690T SIDE PORT

Size | Document Number: Ferrari 7 | Rev: SB

Date: Thursday, August 02, 2007 | Sheet 14 of 47



	LVDS	TMDS
I2C_CLK	I2C_CLK	I2C_CLK
I2C_DATA	I2C_DATA	
DDC_DATA		DDC_DATA

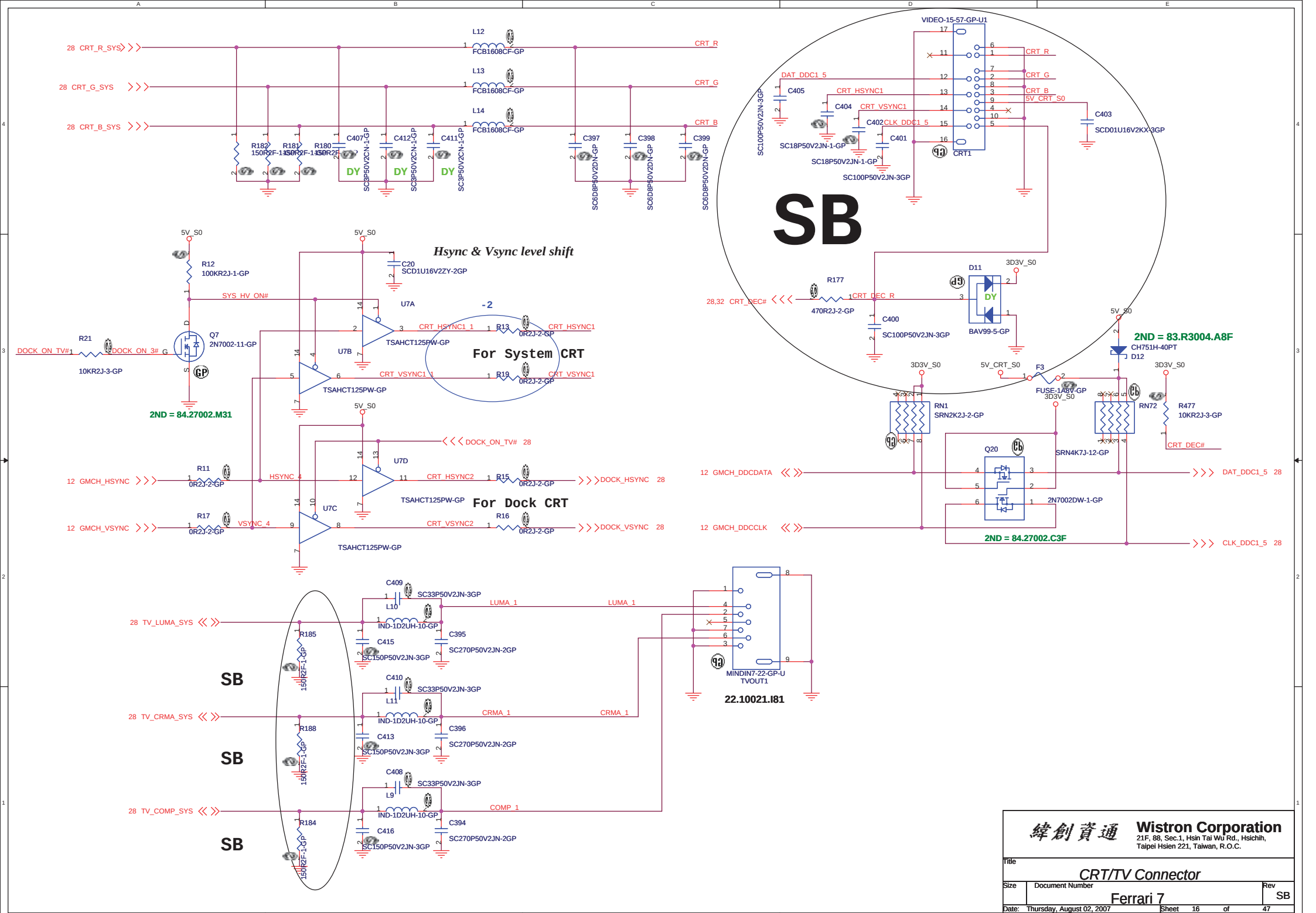
LAYOUT

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN & LED

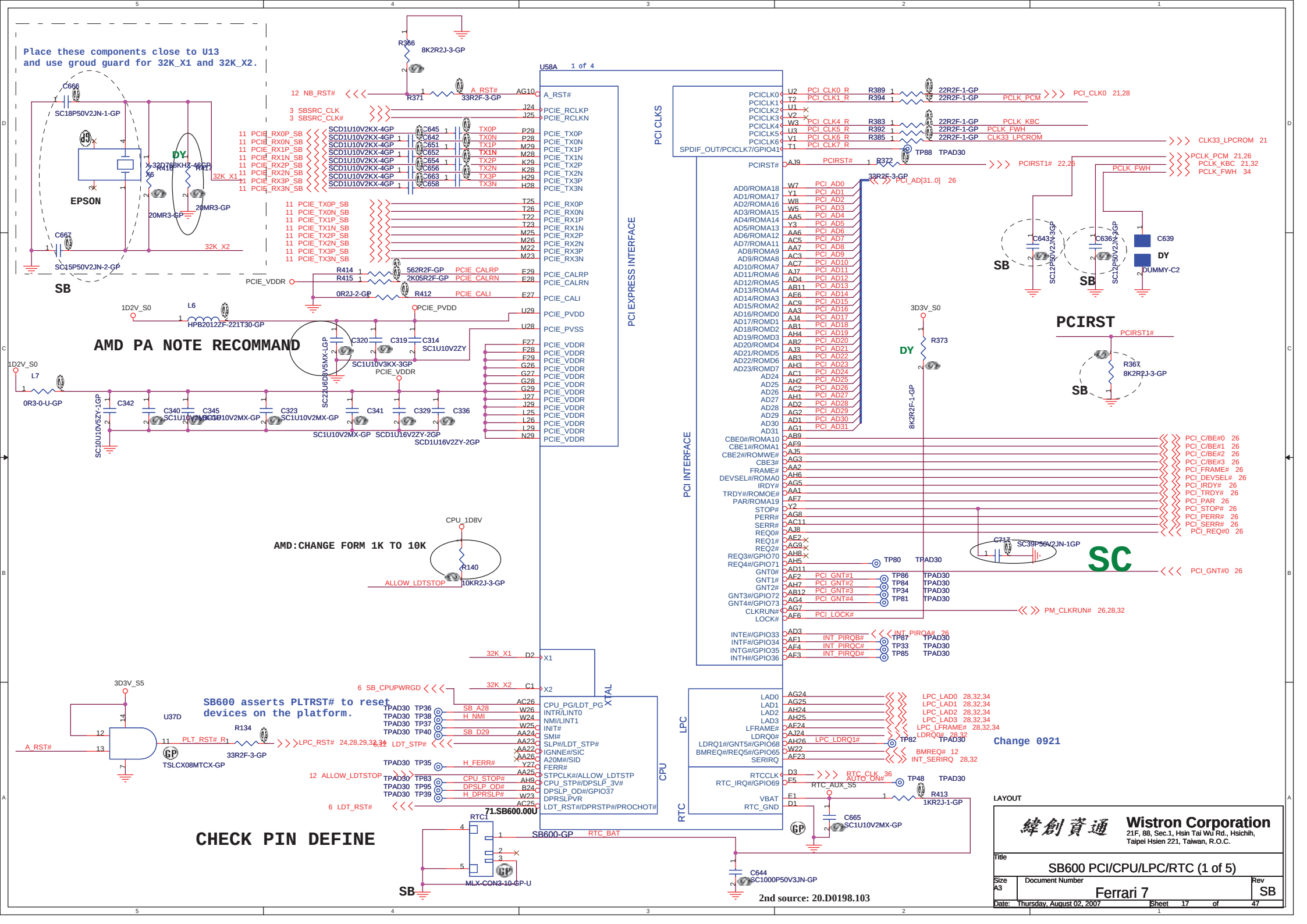
Size | Document Number: Ferrari 7 | Rev: SB

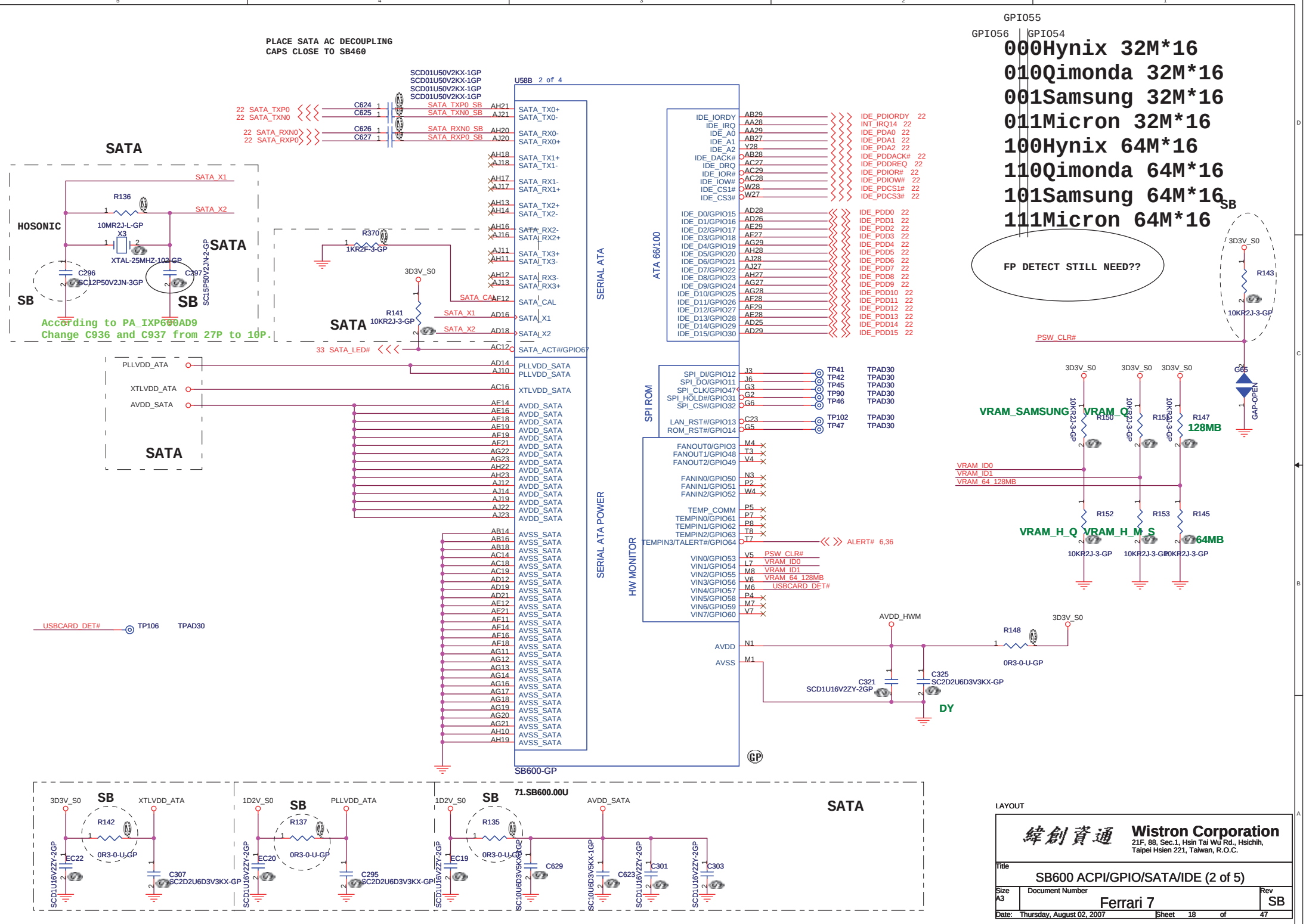
Date: Thursday, August 02, 2007 | Sheet 15 of 47

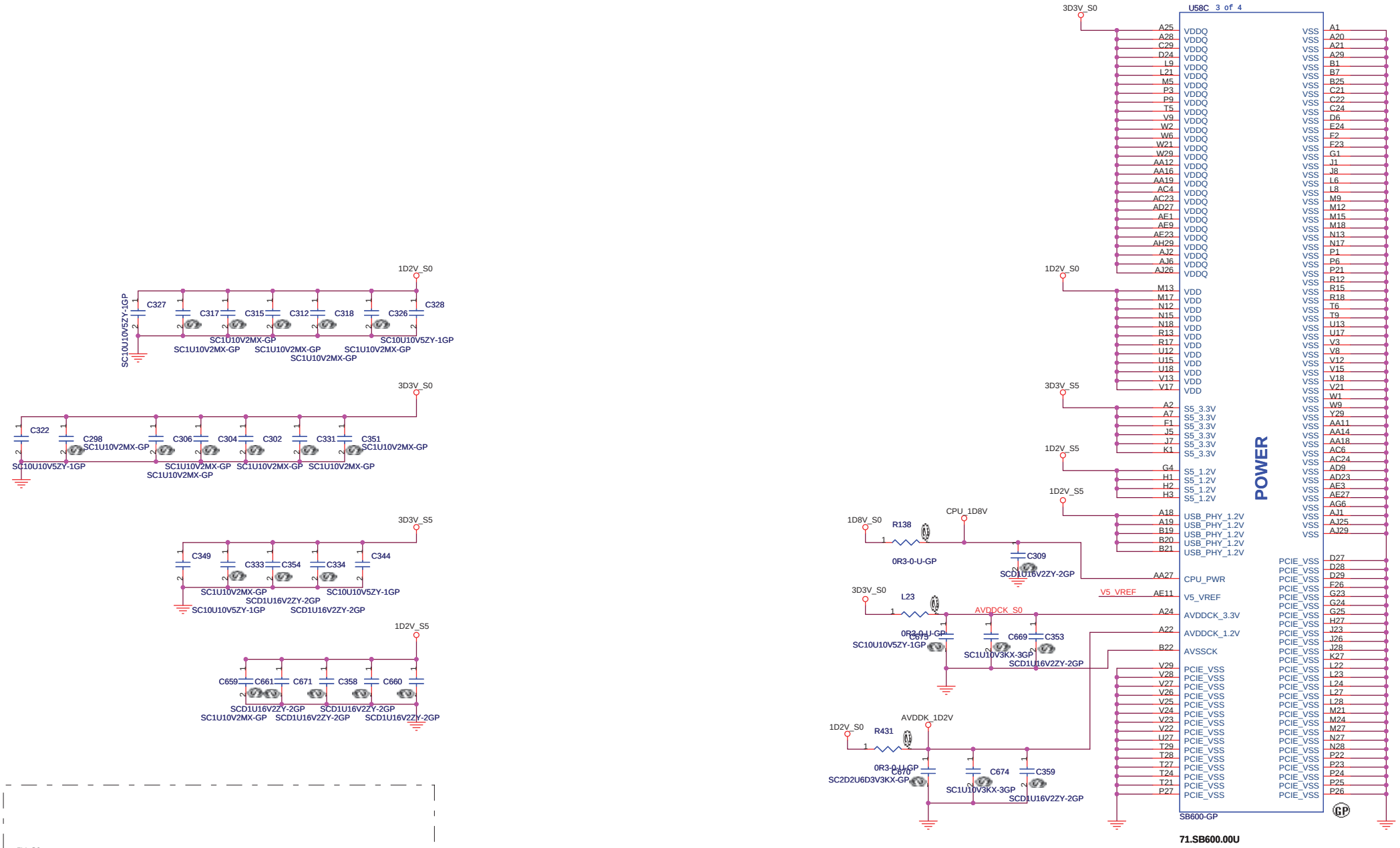


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CRT/TV Connector		
Size	Document Number	Rev
	Ferrari 7	SB
Date: Thursday, August 02, 2007	Sheet 16 of 47	


Place these components close to U13
and use groud guard for 32K_X1 and 32K_X2.
AMD PA NOTE RECOMMAND
AMD:CHANGE FORM 1K TO 10K
SB600 asserts PLTRST# to reset
devices on the platform.
CHECK PIN DEFINE
PCIRST
SC
Change 0921
U58A 1 of 4
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
XTAL
CPU
LPC
RTC
SB600-GP
71.SB600.00U
2nd source: 20.D0198.103
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
SB600 PCI/CPU/LPC/RTC (1 of 5)
Size A3
Document Number
Ferrari 7
Rev SB
Date: Thursday, August 02, 2007
Sheet 17 of 47


PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB460
SCD01U50V2KX-1GP
SCD01U50V2KX-1GP
SCD01U50V2KX-1GP
SCD01U50V2KX-1GP
SCD01U50V2KX-1GP
U58B 2 of 4
22 SATA_TXP0
22 SATA_TXN0
22 SATA_RXN0
22 SATA_RXP0
C624
C625
C626
C627
SATA_TXP0_SB
SATA_TXN0_SB
SATA_RXN0_SB
SATA_RXP0_SB
SATA
SATA_X1
SATA_X2
R136
10MR2J-L-GP
HOSONIC
X3
XTAL-25MHZ-102-GP
C296
SC12P50V2JN-3GP
C297
SC15P50V2JN-2-GP
SB
SB
SATA
R370
1KR2F-3-GP
3D3V_S0
R141
10KR2J-3-GP
SATA_CAL
SATA_X1
SATA_X2
SATA
According to PA_IXP600AD9
Change C936 and C937 from 27P to 10P.
33 SATA_LED#
SATA_ACT#/GPIO67
PLLVDD_ATA
XTLVDD_ATA
AVDD_SATA
SATA
SERIAL ATA
SERIAL ATA POWER
ATA 66/100
SPI ROM
HW MONITOR
IDE_IORDY
IDE_IRQ
IDE_A0
IDE_A1
IDE_A2
IDE_DACK#
IDE_DRQ
IDE_IOR#
IDE_IOW#
IDE_CS1#
IDE_CS3#
IDE_D0/GPIO15
IDE_D1/GPIO16
IDE_D2/GPIO17
IDE_D3/GPIO18
IDE_D4/GPIO19
IDE_D5/GPIO20
IDE_D6/GPIO21
IDE_D7/GPIO22
IDE_D8/GPIO23
IDE_D9/GPIO24
IDE_D10/GPIO25
IDE_D11/GPIO26
IDE_D12/GPIO27
IDE_D13/GPIO28
IDE_D14/GPIO29
IDE_D15/GPIO30
IDE_PDIORDY 22
INT_IRQ14 22
IDE_PDA0 22
IDE_PDA1 22
IDE_PDA2 22
IDE_PDDACK# 22
IDE_PDDREQ 22
IDE_PDIOR# 22
IDE_PDIOW# 22
IDE_PDCS1# 22
IDE_PDCS3# 22
IDE_PDD0 22
IDE_PDD1 22
IDE_PDD2 22
IDE_PDD3 22
IDE_PDD4 22
IDE_PDD5 22
IDE_PDD6 22
IDE_PDD7 22
IDE_PDD8 22
IDE_PDD9 22
IDE_PDD10 22
IDE_PDD11 22
IDE_PDD12 22
IDE_PDD13 22
IDE_PDD14 22
IDE_PDD15 22
SPI_DI/GPIO12
SPI_DO/GPIO11
SPI_CLK/GPIO47
SPI_HOLD#/GPIO31
SPI_CS#/GPIO32
LAN_RST#/GPIO13
ROM_RST#/GPIO14
TP41 TPAD30
TP42 TPAD30
TP45 TPAD30
TP90 TPAD30
TP46 TPAD30
TP102 TPAD30
TP47 TPAD30
FANOUT0/GPIO3
FANOUT1/GPIO48
FANOUT2/GPIO49
FANIN0/GPIO50
FANIN1/GPIO51
FANIN2/GPIO52
TEMP_COMM
TEMPIN0/GPIO61
TEMPIN1/GPIO62
TEMPIN2/GPIO63
TEMPIN3/TALERT#/GPIO64
ALERT# 6,36
VIN0/GPIO53
VIN1/GPIO54
VIN2/GPIO55
VIN3/GPIO56
VIN4/GPIO57
VIN5/GPIO58
VIN6/GPIO59
VIN7/GPIO60
PSW_CLR#
VRAM_ID0
VRAM_ID1
VRAM_64_128MB
USBCARD_DET#
USBCARD_DET#
TP106
TPAD30
AVDD
AVSS
AVDD_HWM
R148
0R3-0-U-GP
C321
SCD1U16V2ZY-2GP
C325
SC2D2U6D3V3KX-GP
DY
SB600-GP
GPIO055
GPIO056
GPIO054
000Hynix 32M*16
010Qimonda 32M*16
001Samsung 32M*16
011Micron 32M*16
100Hynix 64M*16
110Qimonda 64M*16
101Samsung 64M*16
111Micron 64M*16
FP DETECT STILL NEED??
SB
3D3V_S0
R143
10KR2J-3-GP
PSW_CLR#
G65
GAP-OPEN
VRAM_SAMSUNG
VRAM_Q
R150
R151
R147
128MB
VRAM_ID0
VRAM_ID1
VRAM_64_128MB
R152
R153
R145
VRAM_H_Q
VRAM_H_M_S
64MB
10KR2J-3-GP
71.SB600.00U
3D3V_S0
SB
XTLVDD_ATA
R142
0R3-0-U-GP
EC22
SCD1U16V2ZY-2GP
C307
SC2D2U6D3V3KX-GP
1D2V_S0
SB
PLLVDD_ATA
R137
0R3-0-U-GP
EC20
SCD1U16V2ZY-2GP
C295
SC2D2U6D3V3KX-GP
1D2V_S0
SB
R135
0R3-0-U-GP
EC19
SCD1U16V2ZY-2GP
C629
SC10U6D3V5KX-GP
AVDD_SATA
C623
SC10U6D3V5KX-1GP
C301
SCD1U16V2ZY-2GP
C303
SCD1U16V2ZY-2GP
SATA
LAYOUT
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
SB600 ACPI/GPIO/SATA/IDE (2 of 5)
Size A3
Document Number
Ferrari 7
Rev
SB
Date: Thursday, August 02, 2007
Sheet 18 of 47



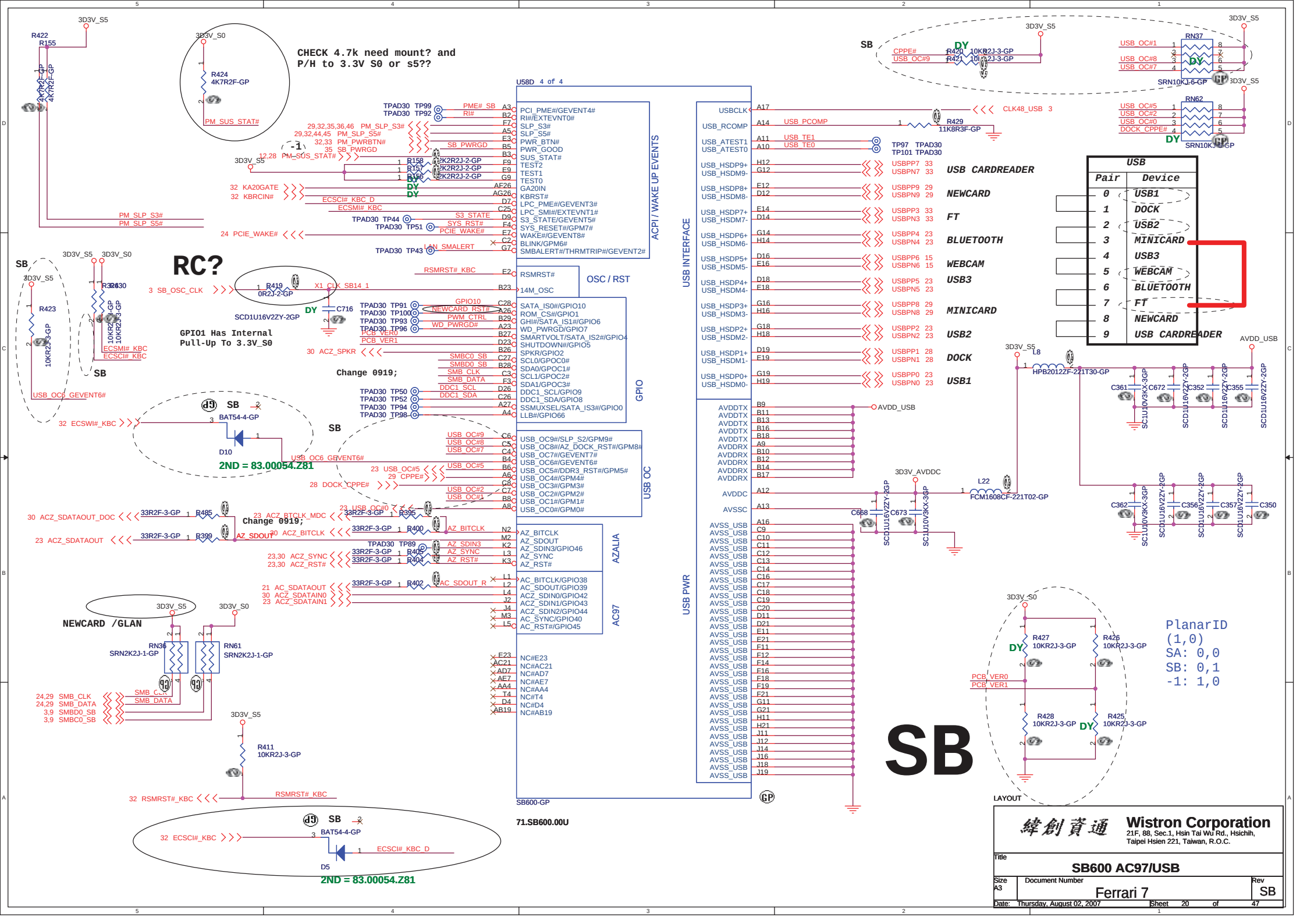
LAYOUT

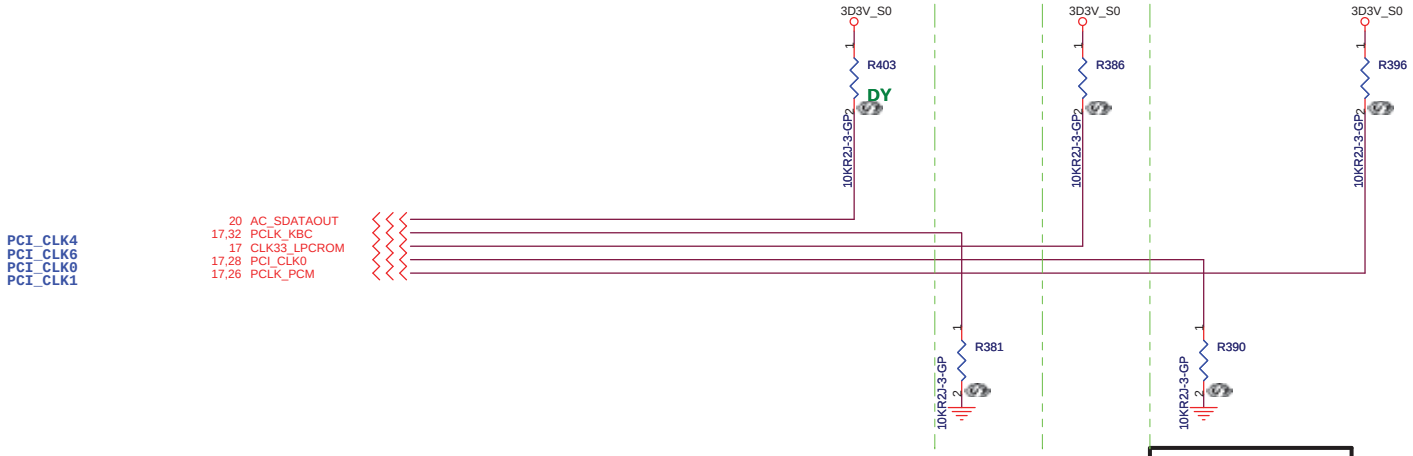
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **SB600 POWER/DECOUPLING**

Size	Document Number	Rev
A3	Ferrari 7	SB

Date: Thursday, August 02, 2007 Sheet 19 of 47


CHECK 4.7k need mount? and
P/H to 3.3V S0 or s5??
RC?
GPIO1 Has Internal
Pull-Up To 3.3V_S0
Change 0919;
Change 0919;
2ND = 83.00054.Z81
2ND = 83.00054.Z81
NEWCARD /GLAN
SB
SB
SB
U58D 4 of 4
ACPI / WAKE UP EVENTS
USB INTERFACE
OSC / RST
GPIO
USB OC
AZALIA
AC97
USB PWR
SB600-GP
71.SB600.00U
USB CARDREADER
NEWCARD
FT
BLUETOOTH
WEBCAM
USB3
MINICARD
USB2
DOCK
USB1
USB
Pair Device
0 USB1
1 DOCK
2 USB2
3 MINICARD
4 USB3
5 WEBCAM
6 BLUETOOTH
7 FT
8 NEWCARD
9 USB CARDREADER
PlanarID
(1,0)
SA: 0,0
SB: 0,1
-1: 1,0
LAYOUT
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
SB600 AC97/USB
Size A3
Document Number
Ferrari 7
Rev SB
Date: Thursday, August 02, 2007
Sheet 20 of 47



REQUIRED SYSTEM STRAPS

				SB600	
	AC_SDOUT	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

SB600 HAS 15K INTERNAL PU FOR PCI_AD[23..28]

DEBUG STRAPS

		PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH		RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW					USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

LAYOUT

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB600 STRAPPING PIN

Size: A3 | Document Number: Ferrari 7 | Rev: SB

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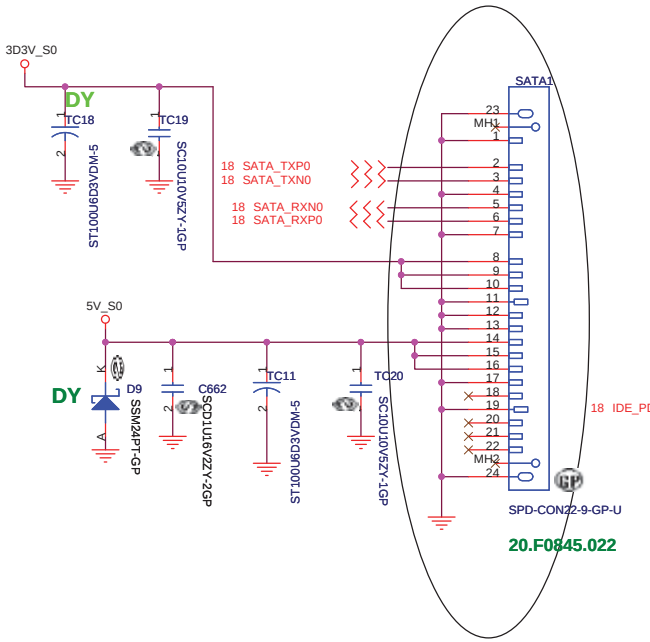
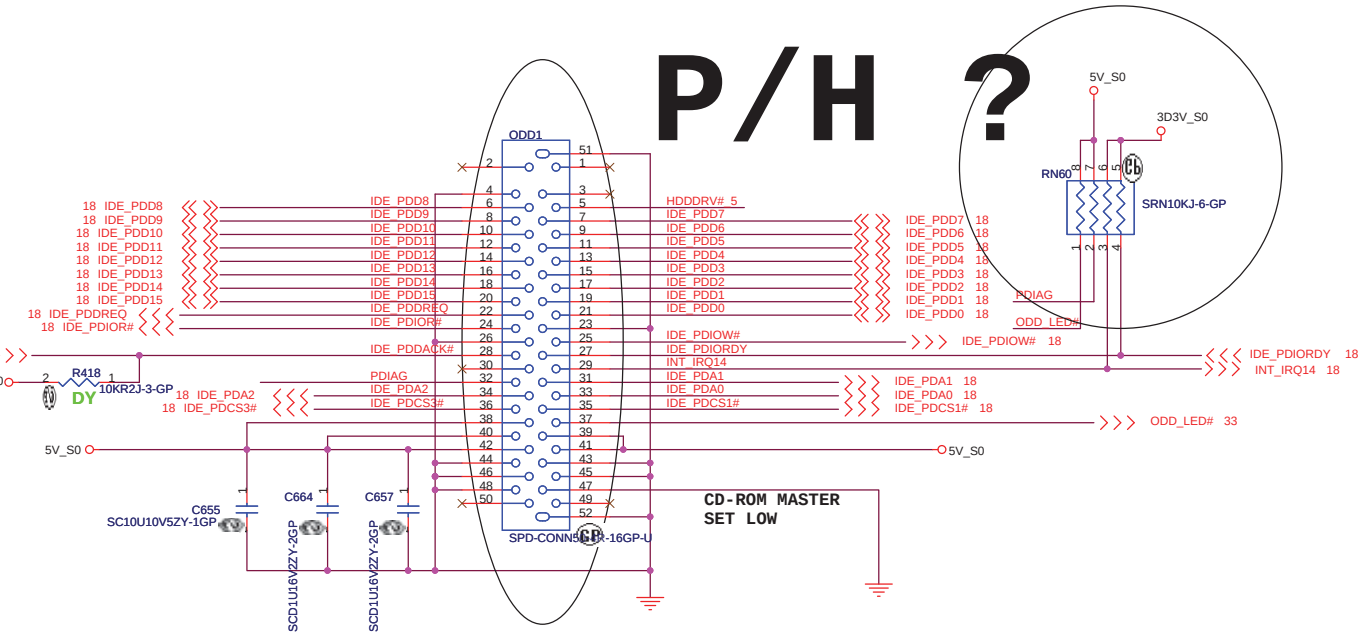
SATA HD Connector



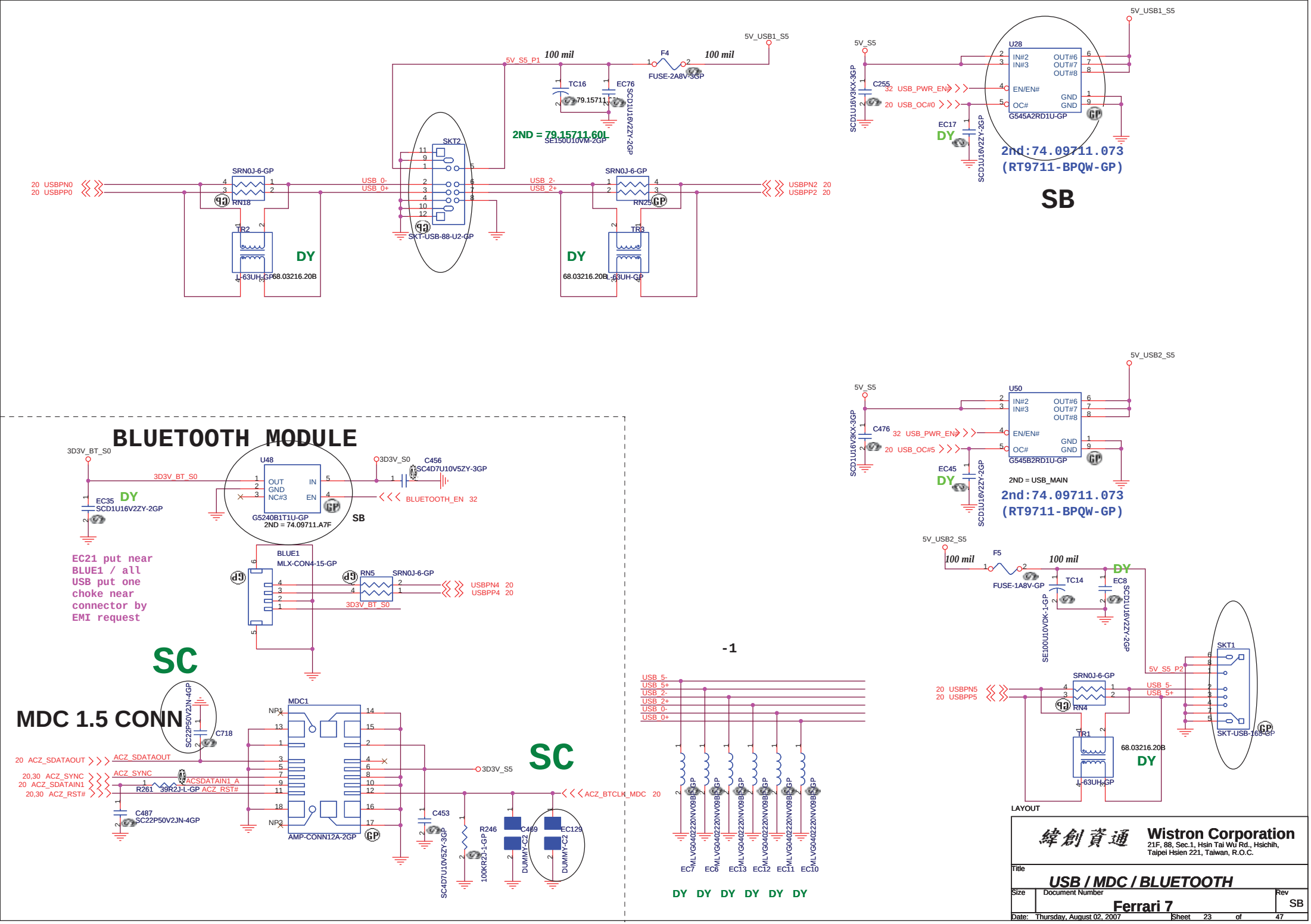
CD-ROM Connector

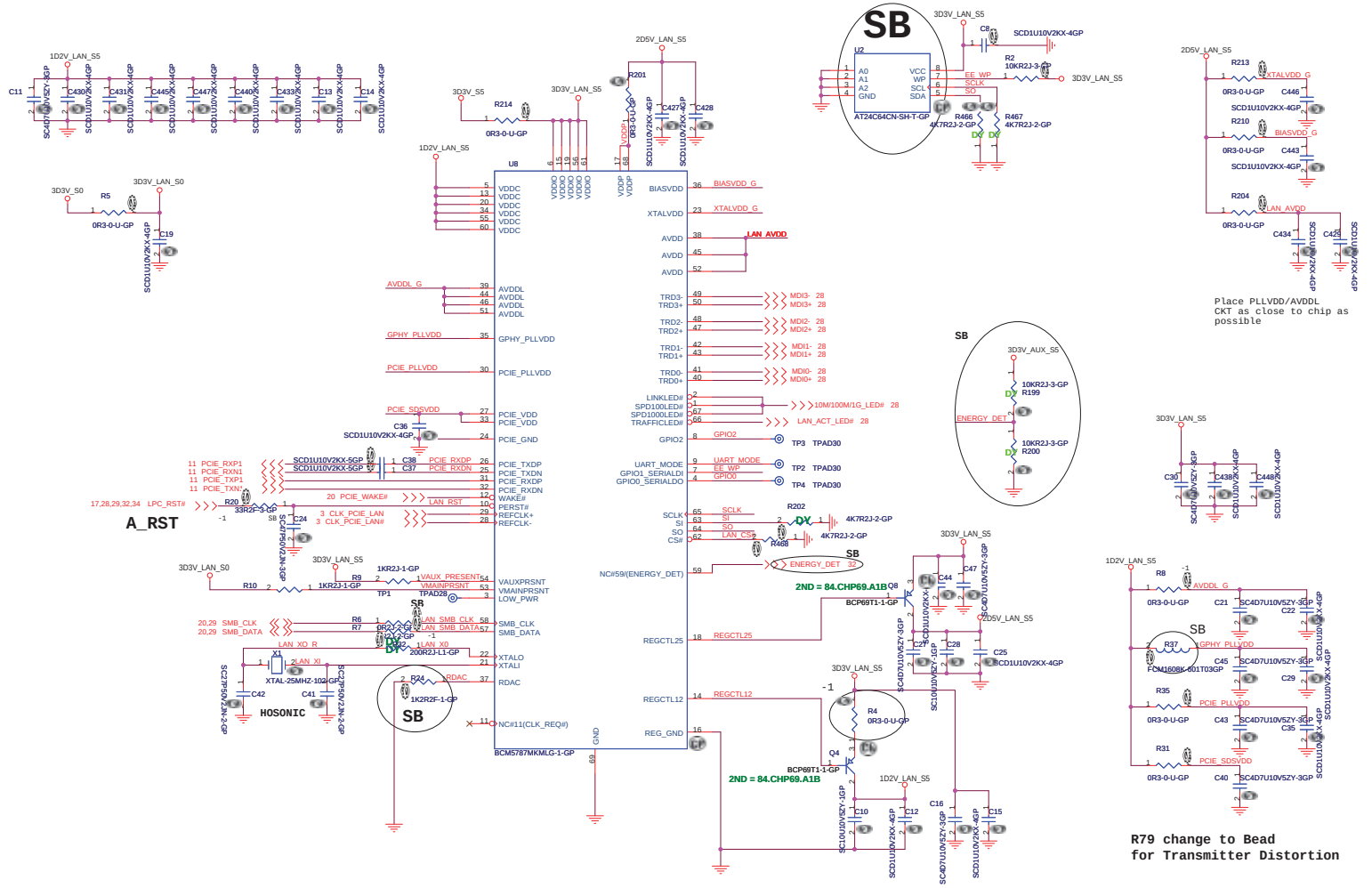


HDD Connector

LAYOUT

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDD and CDROM	
Size	Document Number Ferrari 7	Rev SB
Date: Thursday, August 02, 2007	Sheet 22 of 47	


5V_USB1_S5
5V_S5_P1
100 mil
F4
FUSE-2A8V-3GP
TC16
79.15711
EC76
SCD1U16V2ZY-2GP
2ND = 79.15711.60L
SE150U10VM-2GP
SKT2
SKT-USB-88-U2-GP
20 USBPN0
20 USBPP0
SRN0J-6-GP
RN18
USB_0-
USB_0+
USB_2-
USB_2+
RN25
USBPN2 20
USBPP2 20
TR2
TR3
DY
L-63UH-GP
68.03216.20B
5V_S5
U28
IN#2
IN#3
OUT#6
OUT#7
OUT#8
EN/EN#
OC#
GND
G545A2RD1U-GP
C255
32 USB_PWR_EN#
20 USB_OC#0
SCD1U16V3KX-3GP
EC17
2nd:74.09711.073
(RT9711-BPQW-GP)
SB
5V_USB2_S5
U50
C476
32 USB_PWR_EN#
20 USB_OC#5
SCD1U16V3KX-3GP
EC45
G545B2RD1U-GP
2ND = USB_MAIN
2nd:74.09711.073
(RT9711-BPQW-GP)
BLUETOOTH MODULE
3D3V_BT_S0
EC35
SCD1U16V2ZY-2GP
U48
OUT
GND
NC#3
IN
EN
G5240B1T1U-GP
2ND = 74.09711.A7F
C456
SC4D7U10V5ZY-3GP
BLUETOOTH_EN 32
EC21 put near BLUE1 / all USB put one choke near connector by EMI request
BLUE1
MLX-CON4-15-GP
RN5
SRN0J-6-GP
USBPN4 20
USBPP4 20
SC
MDC 1.5 CONN
SC22P50V2JN-4GP
C718
MDC1
NP1
NP2
AMP-CONN12A-2GP
20 ACZ_SDATAOUT
ACZ_SDATAOUT
20,30 ACZ_SYNC
20 ACZ_SDATAIN1
20,30 ACZ_RST#
ACZ_SYNC
ACSDATAIN1_A
R261
39R2J-L-GP
ACZ_RST#
C487
SC22P50V2JN-4GP
3D3V_S5
C453
SC4D7U10V52Y-3GP
R246
100KR2J-1-GP
C489
DUMMY-C2
EC129
DUMMY-C2
ACZ_BTCLK_MDC 20
-1
USB_5-
USB_5+
USB_2-
USB_2+
USB_0-
USB_0+
EC7
EC6
EC13
EC12
EC11
EC10
MLVG0402220NV09B-GP
DY DY DY DY DY DY
5V_USB2_S5
100 mil
F5
FUSE-1A8V-GP
TC14
SE100U10VDK-1-GP
EC8
SCD1U16V2ZY-2GP
SKT1
5V_S5_P2
20 USBPN5
20 USBPP5
SRN0J-6-GP
RN4
USB_5-
USB_5+
TR1
68.03216.20B
L-63UH-GP
SKT-USB-163-GP
LAYOUT
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
USB / MDC / BLUETOOTH
Size
Document Number
Ferrari 7
Rev
SB
Date: Thursday, August 02, 2007
Sheet 23 of 47



LAYOUT

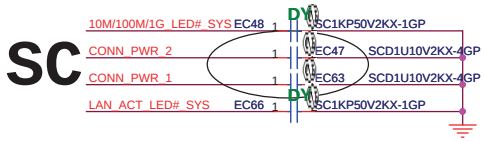
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

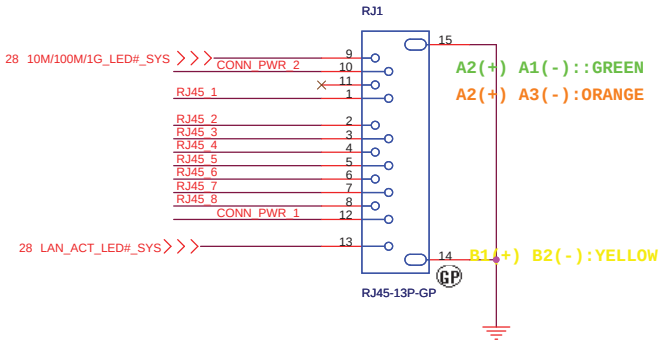
Title: **BCM5787MKMLG**

Size	Document Number	Rev
A2	Ferrari 7	SB

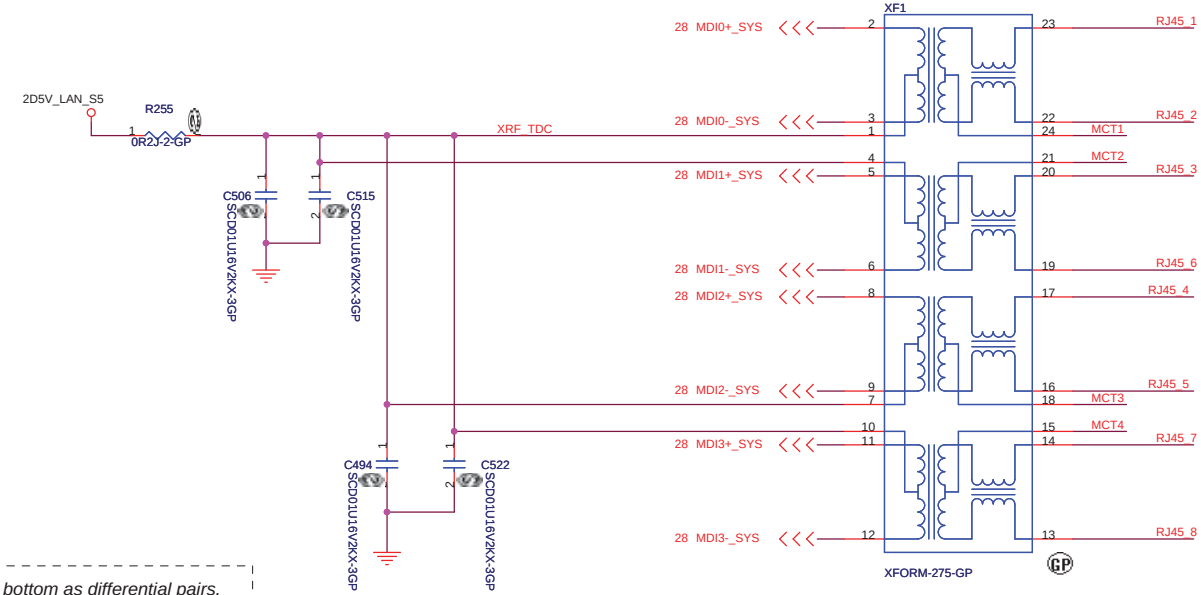
Date: Thursday, August 02, 2007 Sheet 24 of 47

LAN Connector

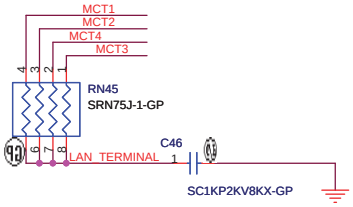




GIGA Lan Transformer



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

LAYOUT

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

Size: A3 | Document Number: **Ferrari 7** | Rev: **SB**

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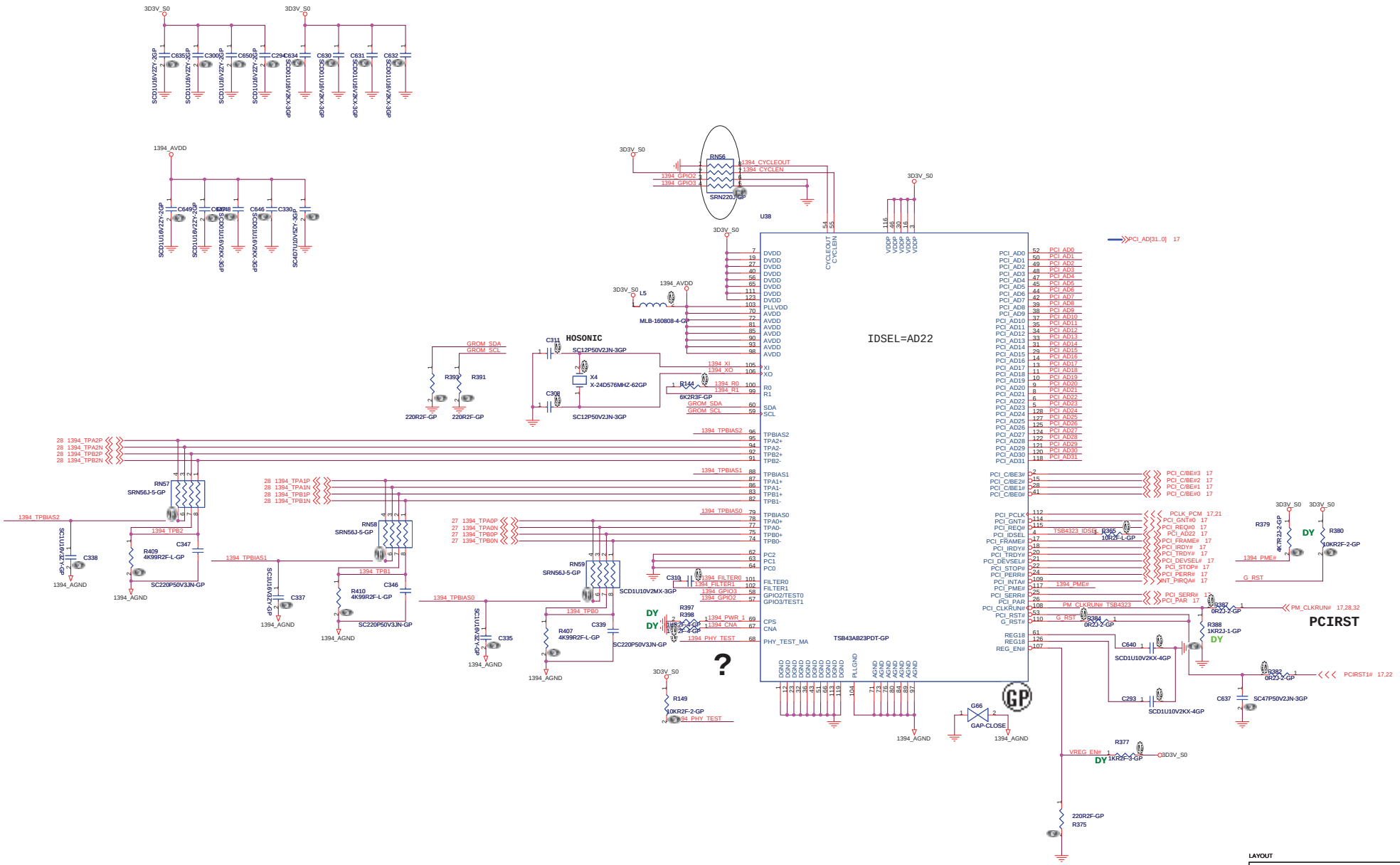

LAYOUT

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *TSB4323 (1 of 1)*

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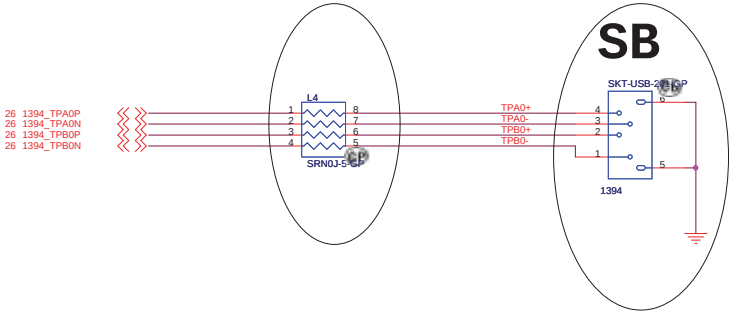
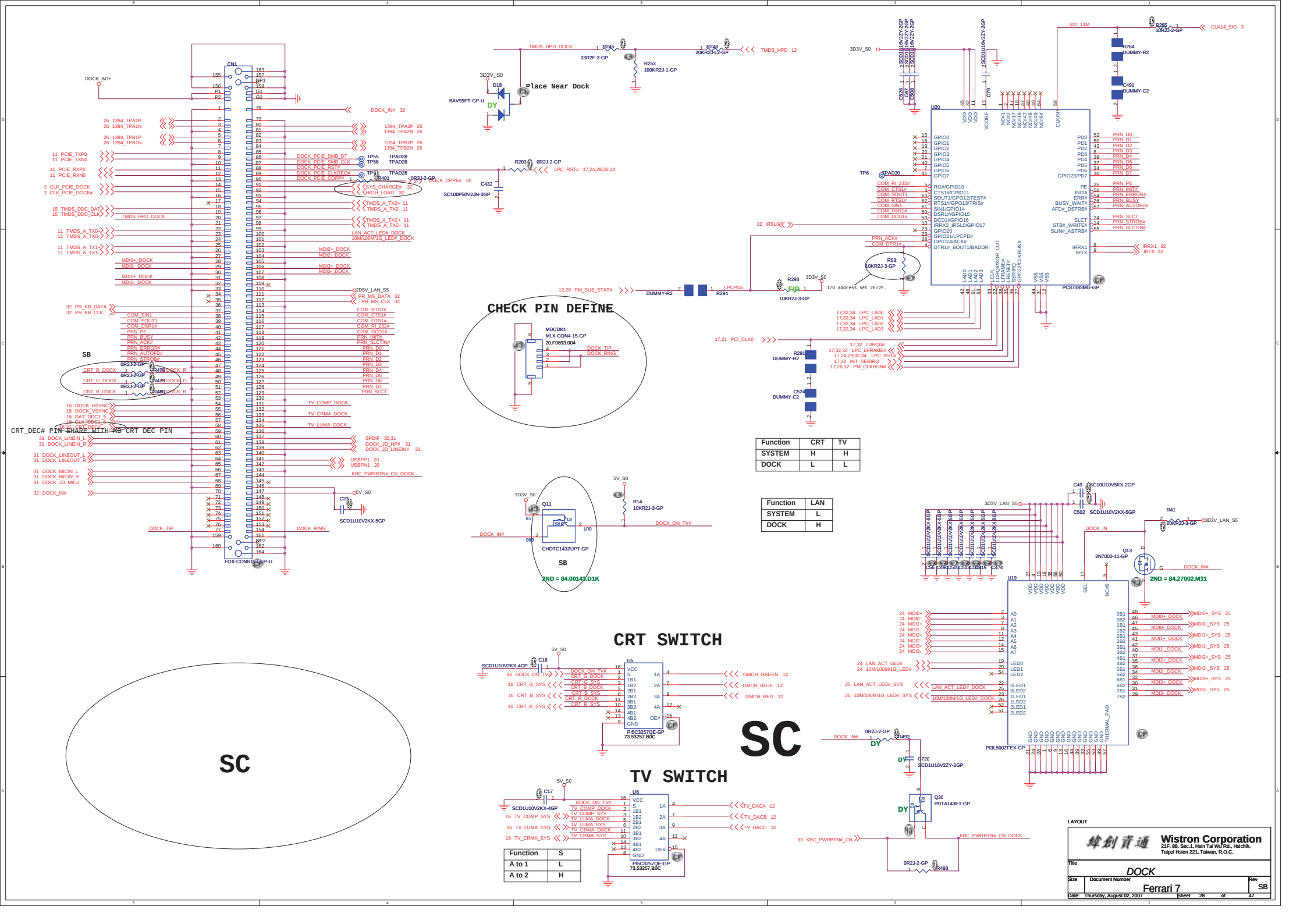
Date: Thursday, August 02, 2007 | Sheet 26 of 47

1394 Connector



LAYOUT

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*PCMCIA / 1394 / CARD READER*
Size / Document Number	Ferrari 7
Rev	SB
Date: Thursday, August 02, 2007	Sheet 27 of 47


CN1
FOX-CONN1-GP-U
CHECK PIN DEFINE
MDCDK1
MLX-CON4-15-GP
20.F0693.004
SB
CRT_DEC# PIN SHARE WITH MB CRT DEC PIN
Place Near Dock
U20
PC87383MG-GP
U19
PI3L500ZFEX-GP
Q30
PDTA143ET-GP
Q11
CHDTC143UPT-GP
2ND = 84.00143.D1K
2ND = 84.27002.M31
CRT SWITCH
U5
PI5C3257QE-GP
73.53257.B0C
TV SWITCH
U6
SC
SC
Function | CRT | TV
SYSTEM | H | H
DOCK | L | L
Function | LAN
SYSTEM | L
DOCK | H
Function | S
A to 1 | L
A to 2 | H
LAYOUT
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DOCK
Size
Document Number
Ferrari 7
Rev
SB
Date: Thursday, August 02, 2007
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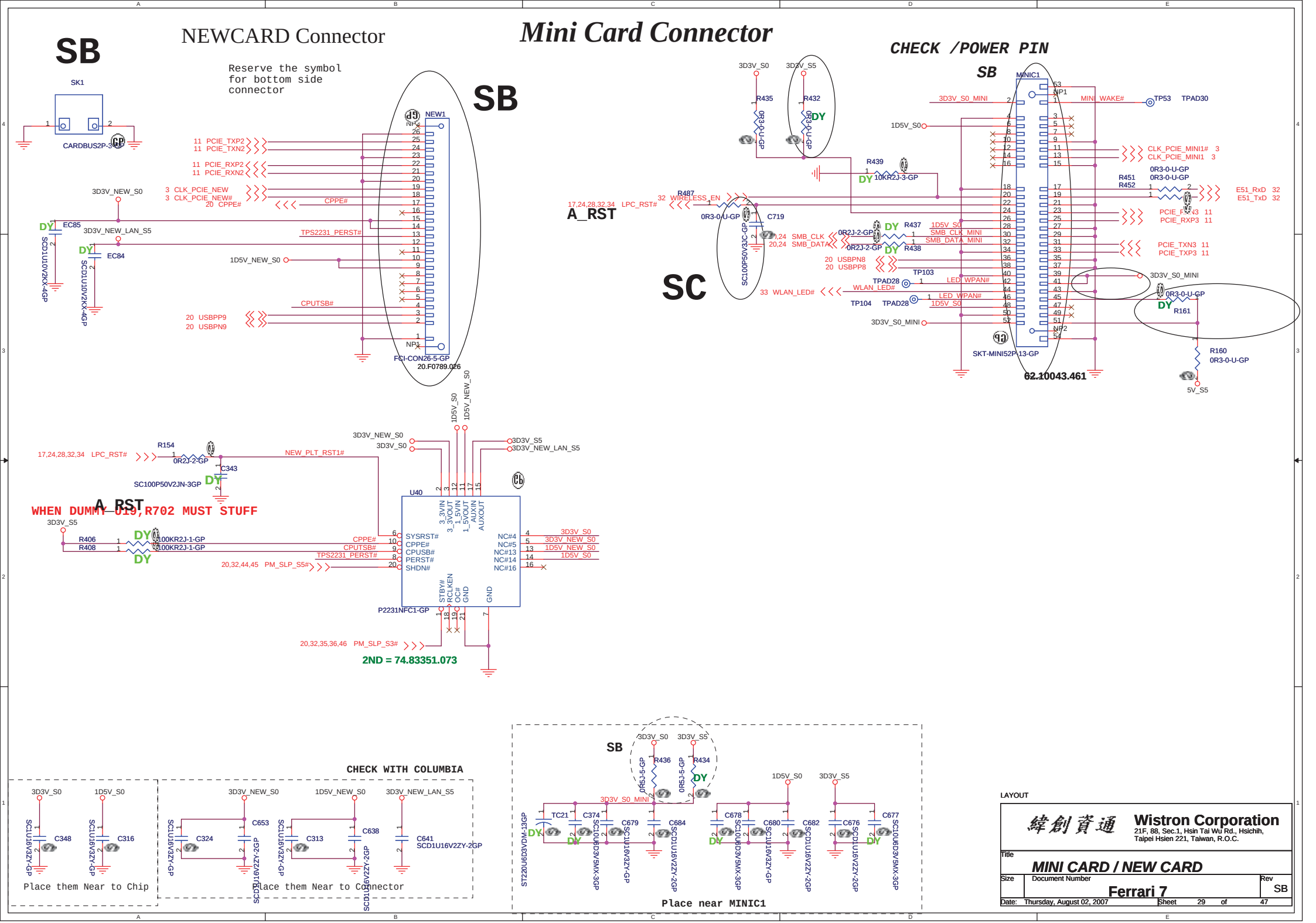
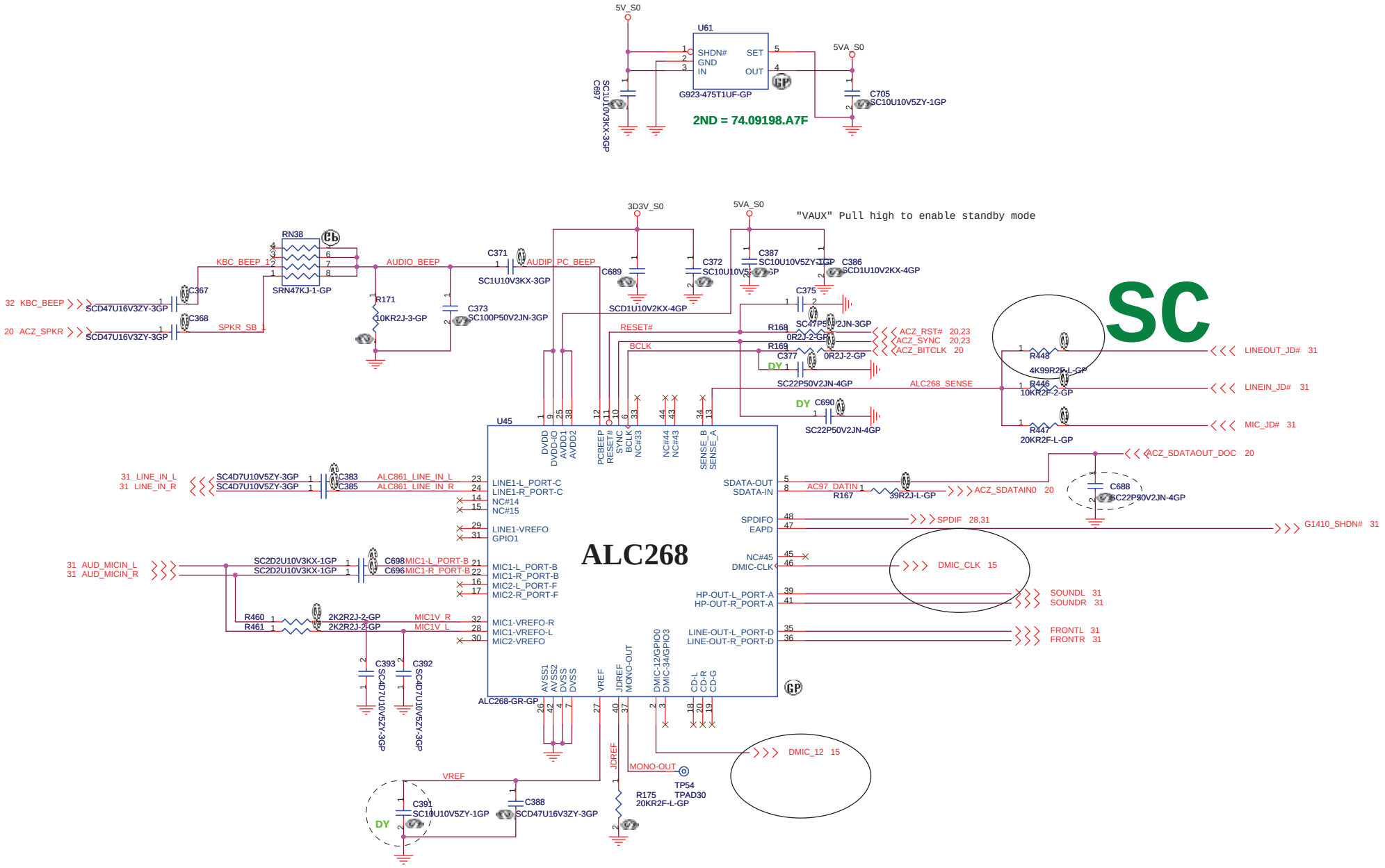
NEWCARD Connector

Mini Card Connector



LAYOUT

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	MINI CARD / NEW CARD
Size	Document Number: Ferrari 7 — Rev: SB
Date: Thursday, August 02, 2007	Sheet 29 of 47



LAYOUT

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*AZALIA CODEC - ALC268*	
Size	Document Number Ferrari 7	Rev SB
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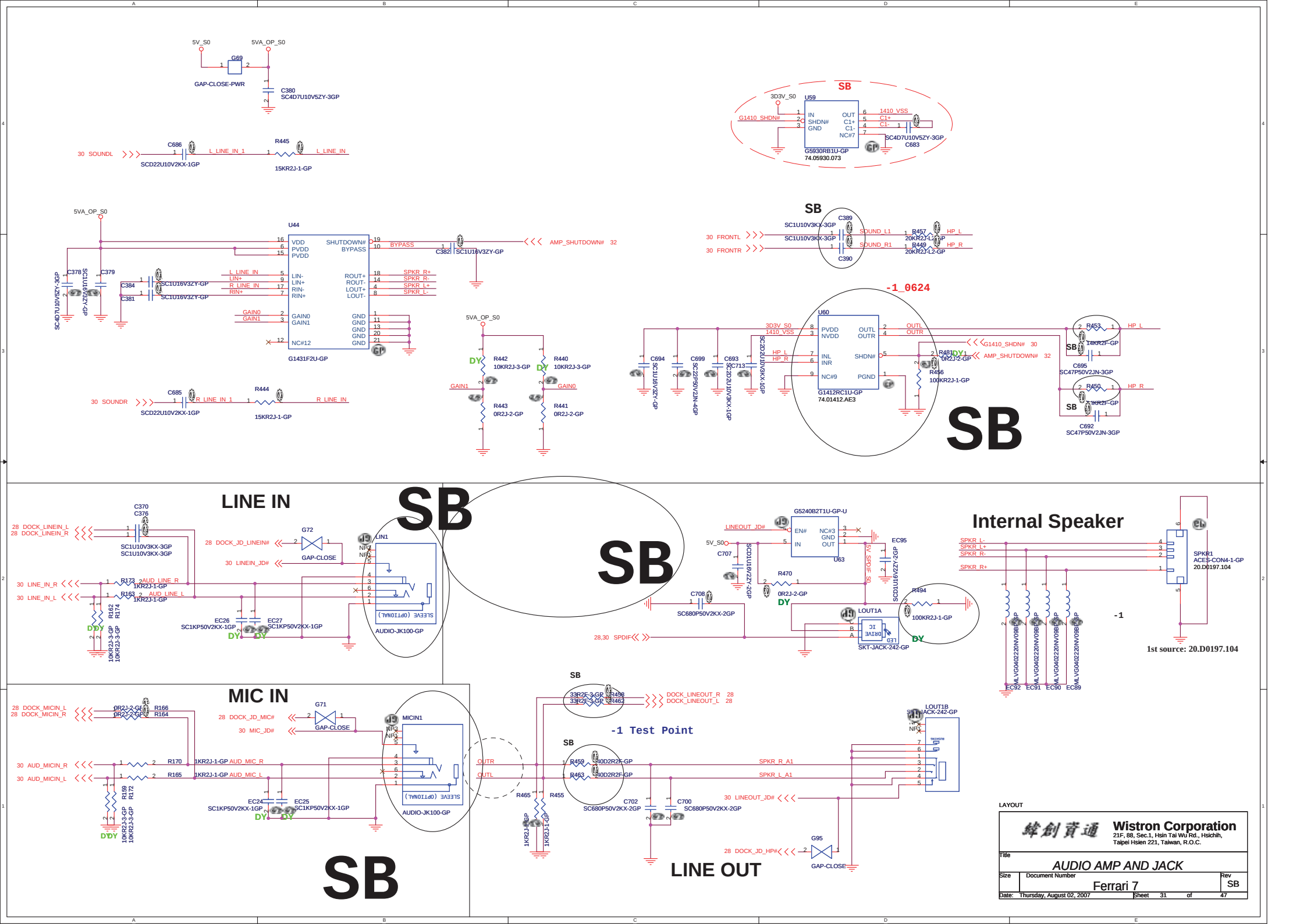
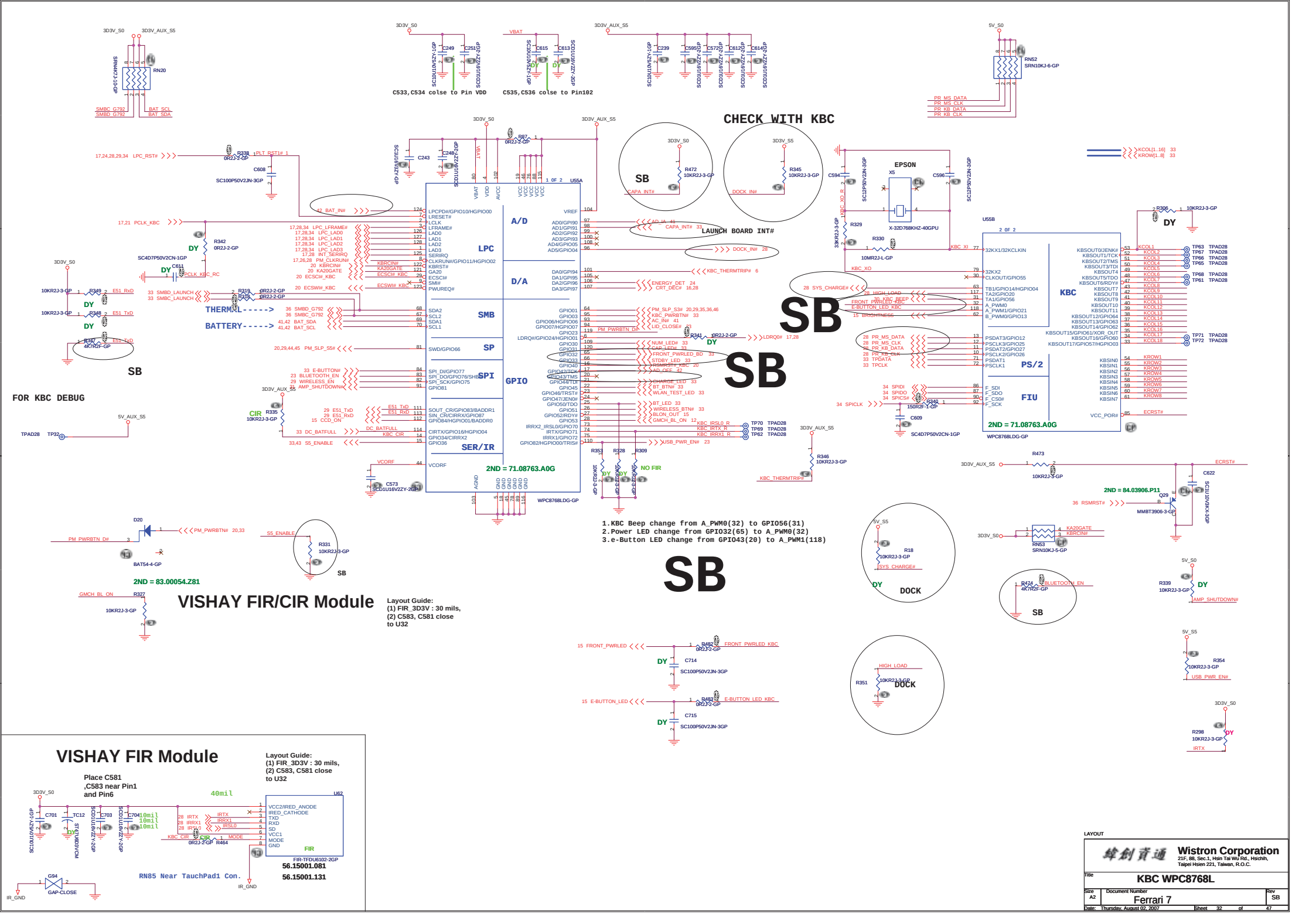

5V_S0
5VA_OP_S0
G69
GAP-CLOSE-PWR
C380
SC4D7U10V5ZY-3GP
30 SOUNDL
C686
SCD22U10V2KX-1GP
L_LINE_IN_1
R445
15KR2J-1-GP
L_LINE_IN
SB
3D3V_S0
U59
G1410_SHDN#
IN
SHDN#
GND
OUT
C1+
C1-
NC#7
1410_VSS
C1+
C1-
SC4D7U10V5ZY-3GP
C683
G5930RB1U-GP
74.05930.073
5VA_OP_S0
U44
VDD
PVDD
PVDD
SHUTDOWN#
BYPASS
BYPASS
C382
SC1U16V3ZY-GP
AMP_SHUTDOWN# 32
C378
SC4D7U10V5ZY-3GP
C379
SC1U16V3ZY-GP
C384
C381
SC1U16V3ZY-GP
L_LINE_IN
LIN+
R_LINE_IN
RIN+
LIN-
LIN+
RIN-
RIN+
ROUT+
ROUT-
LOUT+
LOUT-
SPKR_R+
SPKR_R-
SPKR_L+
SPKR_L-
GAIN0
GAIN1
GAIN0
GAIN1
NC#12
GND
GND
GND
GND
GND
G1431F2U-GP
5VA_OP_S0
DY
R442
10KR2J-3-GP
DY
R440
10KR2J-3-GP
GAIN1
GAIN0
R443
0R2J-2-GP
R441
0R2J-2-GP
30 SOUNDR
C685
SCD22U10V2KX-1GP
R_LINE_IN_1
R444
15KR2J-1-GP
R_LINE_IN
SB
30 FRONTL
30 FRONTR
C389
SC1U10V3KX-3GP
SC1U10V3KX-3GP
C390
SOUND_L1
SOUND_R1
R457
20KR2J-L2-GP
R449
20KR2J-L2-GP
HP_L
HP_R
-1_0624
U60
3D3V_S0
1410_VSS
PVDD
NVDD
INL
INR
NC#9
OUTL
OUTR
SHDN#
PGND
G1412RC1U-GP
74.01412.AE3
C694
SC1U16V2ZY-GP
C699
SC22P50V2JN-4GP
C693
SC2D2U10V3KX-1GP
C713
SC2D2U10V3KX-1GP
HP_L
HP_R
OUTL
OUTR
G1410_SHDN# 30
R481
0R2J-2-GP
AMP_SHUTDOWN# 32
R496
100KR2J-1-GP
R453
14KR2F-GP
SB
C695
SC47P50V2JN-3GP
R450
14KR2F-GP
SB
C692
SC47P50V2JN-3GP
HP_L
HP_R
SB
LINE IN
SB
28 DOCK_LINEIN_L
28 DOCK_LINEIN_R
C370
C376
SC1U10V3KX-3GP
SC1U10V3KX-3GP
28 DOCK_JD_LINEIN#
30 LINEIN_JD#
G72
GAP-CLOSE
LIN1
30 LINE_IN_R
30 LINE_IN_L
R173
1KR2J-1-GP
AUD_LINE_R
R163
1KR2J-1-GP
AUD_LINE_L
R162
R174
10KR2J-3-GP
10KR2J-3-GP
EC26
SC1KP50V2KX-1GP
EC27
SC1KP50V2KX-1GP
SLEEVE (OPTIONAL)
AUDIO-JK100-GP
SB
LINEOUT_JD#
G5240B2T1U-GP-U
EN#
IN
NC#3
GND
OUT
U63
5V_S0
C707
SC1U16V2ZY-3GP
EC95
5V_SPDIF_SB
SCD1U16V2ZY-2GP
R470
0R2J-2-GP
DY
C708
SC680P50V2KX-2GP
28,30 SPDIF
LOUT1A
SKT-JACK-242-GP
R494
100KR2J-1-GP
DY
Internal Speaker
SPKR_L-
SPKR_L+
SPKR_R-
SPKR_R+
SPKR1
ACES-CON4-1-GP
20.D0197.104
-1
EC92
EC91
EC90
EC89
1st source: 20.D0197.104
MIC IN
28 DOCK_MICIN_L
28 DOCK_MICIN_R
0R2J-2-GP
0R2J-2-GP
R166
R164
28 DOCK_JD_MIC#
30 MIC_JD#
G71
GAP-CLOSE
MICIN1
30 AUD_MICIN_R
30 AUD_MICIN_L
R170
1KR2J-1-GP
AUD_MIC_R
R165
1KR2J-1-GP
AUD_MIC_L
R159
R172
10KR2J-3-GP
10KR2J-3-GP
EC24
SC1KP50V2KX-1GP
EC25
SC1KP50V2KX-1GP
SLEEVE (OPTIONAL)
AUDIO-JK100-GP
SB
SB
33R2F-3-GP
R498
33R2F-3-GP
R462
DOCK_LINEOUT_R 28
DOCK_LINEOUT_L 28
-1 Test Point
SB
OUTR
OUTL
R465
1KR2J-1-GP
R455
1KR2J-1-GP
R459
10D2R2F-GP
R463
10D2R2F-GP
SPKR_R_A1
SPKR_L_A1
C702
SC680P50V2KX-2GP
C700
SC680P50V2KX-2GP
30 LINEOUT_JD#
LOUT1B
JACK-242-GP
28 DOCK_JD_HP#
G95
GAP-CLOSE
LINE OUT
LAYOUT
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO AMP AND JACK
Size
Document Number
Ferrari 7
Rev
SB
Date: Thursday, August 02, 2007
Sheet 31 of 47


CHECK WITH KBC
C533,C534 colse to Pin VDD
C535,C536 colse to Pin102
LAUNCH BOARD INT#
SB
FOR KBC DEBUG
THERM-L----->
BATTERY----->
2ND = 71.08763.A0G
WPC8768LDG-GP
KBC
PS/2
FIU
LPC
SMB
SP
SPI
GPIO
SER/IR
A/D
D/A
EPSON
X-32D768KHZ-40GPU
NO FIR
1.KBC Beep change from A_PWM0(32) to GPIO56(31)
2.Power LED change from GPIO32(65) to A_PWM0(32)
3.e-Button LED change from GPIO43(20) to A_PWM1(118)
2ND = 83.00054.Z81
VISHAY FIR/CIR Module
Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close
to U32
2ND = 84.03906.P11
DOCK
VISHAY FIR Module
Place C581
,C583 near Pin1
and Pin6
40mil
RN85 Near TauchPad1 Con.
56.15001.081
56.15001.131
LAYOUT
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC WPC8768L
Size A2
Document Number
Ferrari 7
Rev SB
Date: Thursday, August 02, 2007
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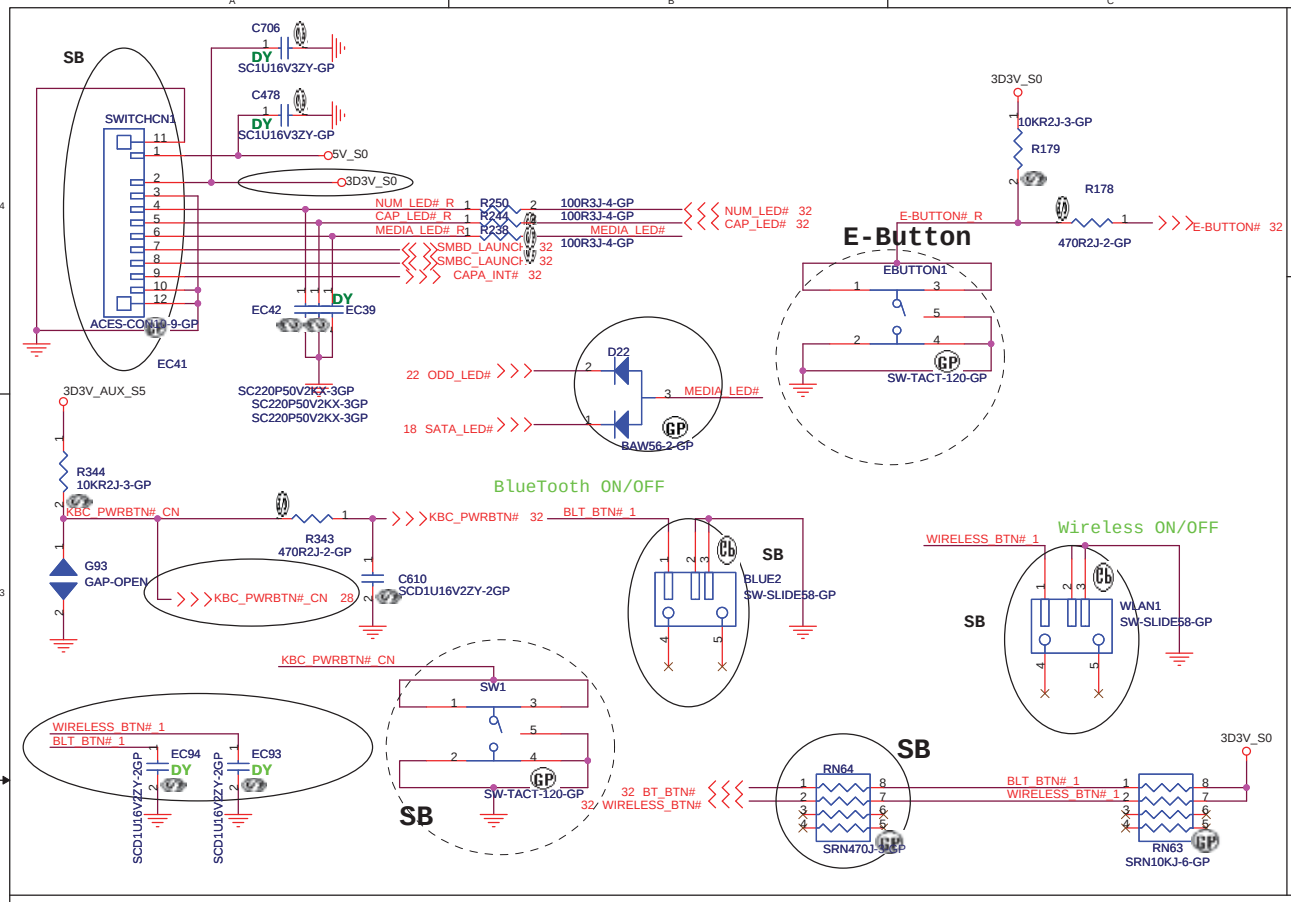
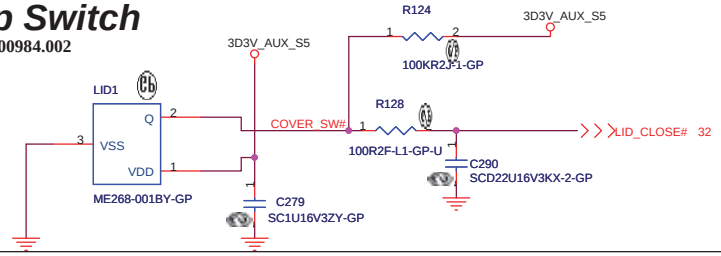
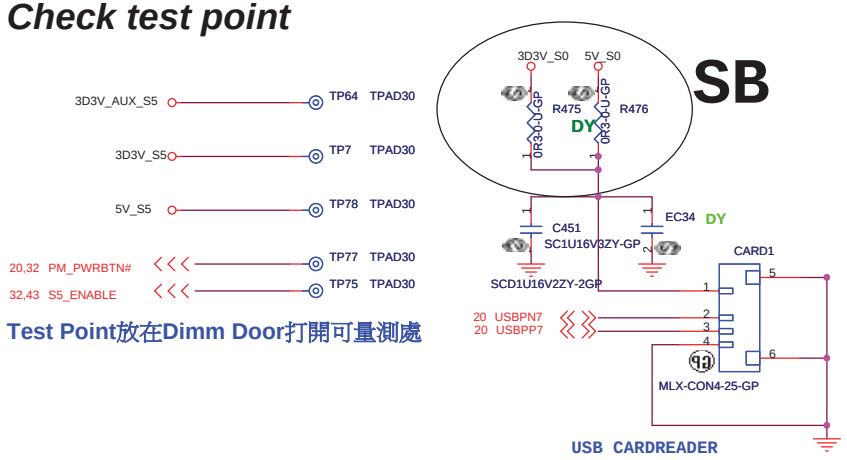


Cover Up Switch

2nd source:20.F00984.002



Check test point

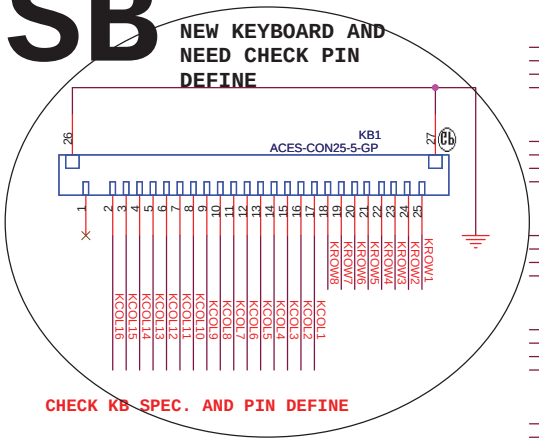


Test Point放在Dimm Door打開可量測處

USB CARDREADER

SB

NEW KEYBOARD AND NEED CHECK PIN DEFINE

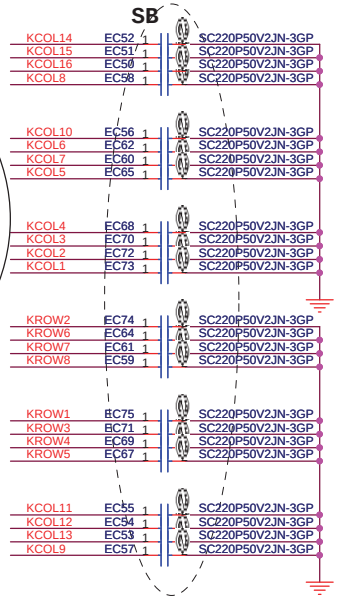


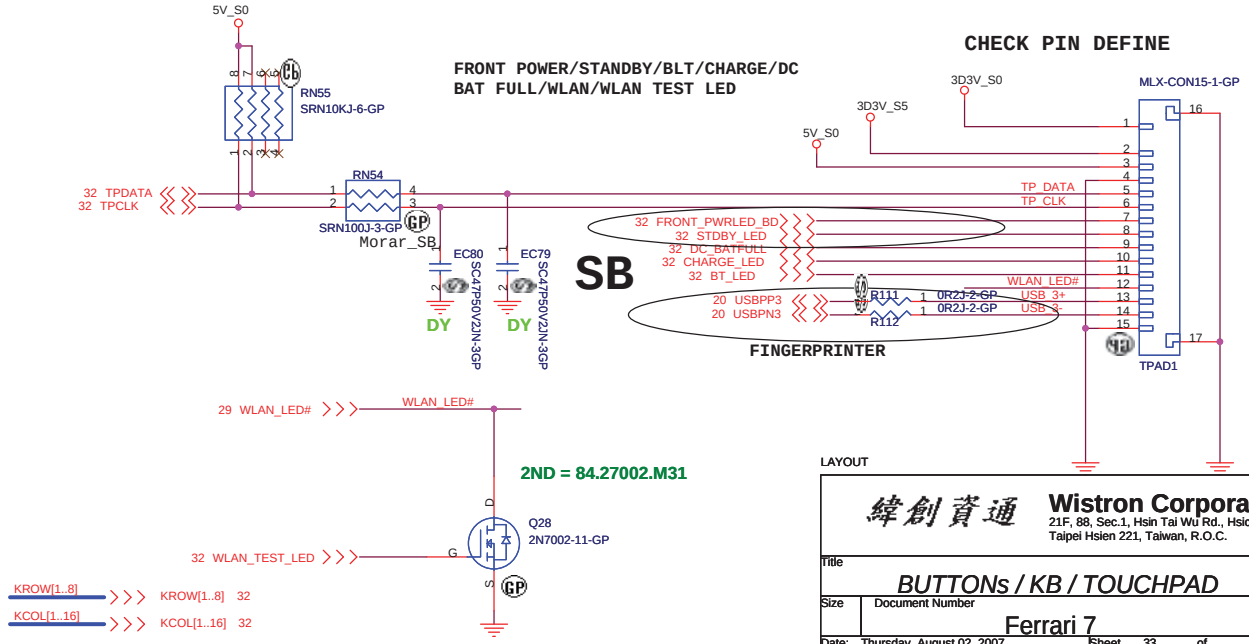
CHECK KB SPEC. AND PIN DEFINE

Internal KeyBoard CONN

1 25

EMI Bypass cap.





LAYOUT

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*BUTTONs / KB / TOUCHPAD*
Size / Document Number	Ferrari 7
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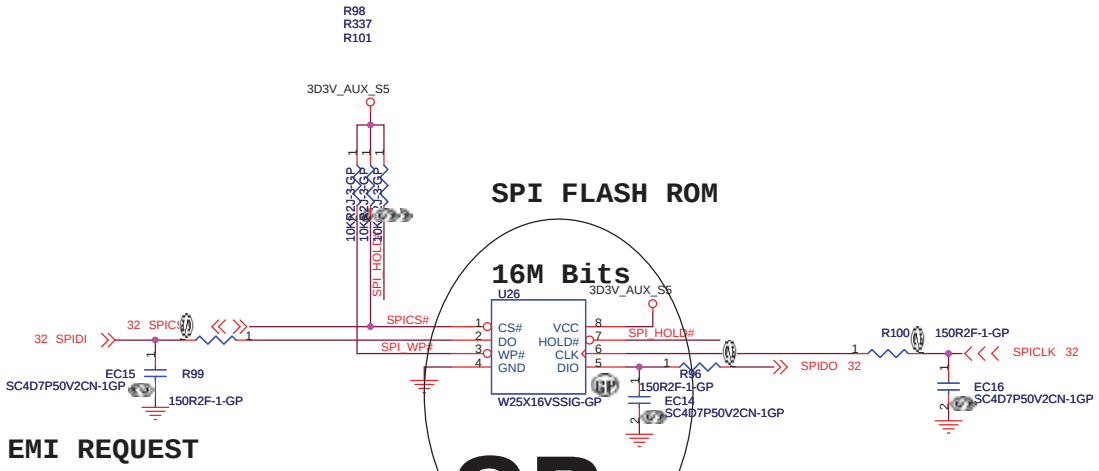
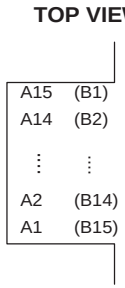
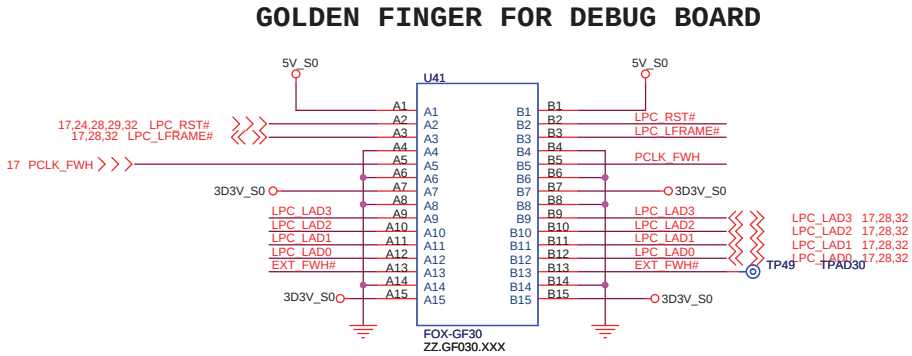


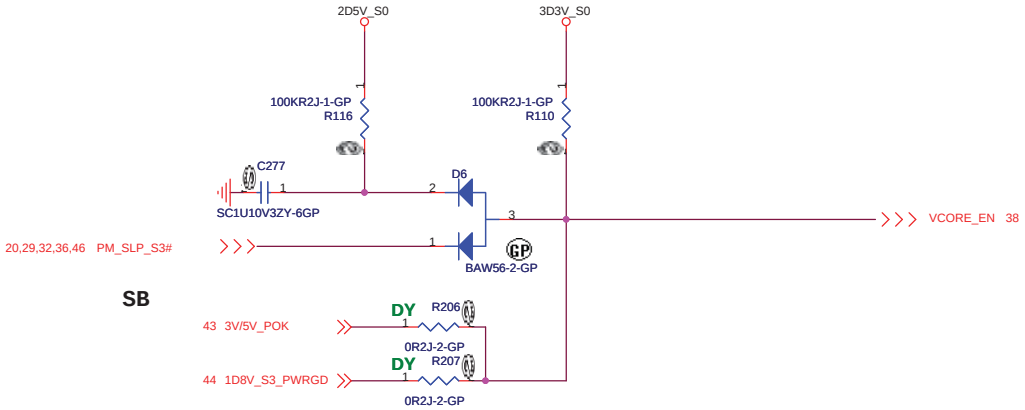
EMI REQUEST



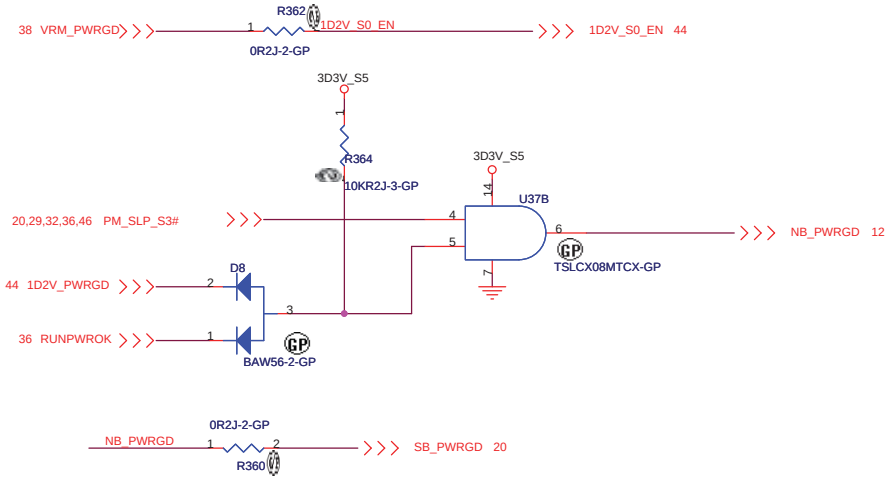


LAYOUT

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	BIOS
Size A3	Document Number: Ferrari 7 — Rev SB
Date: Thursday, August 02, 2007	Sheet 34 of 47

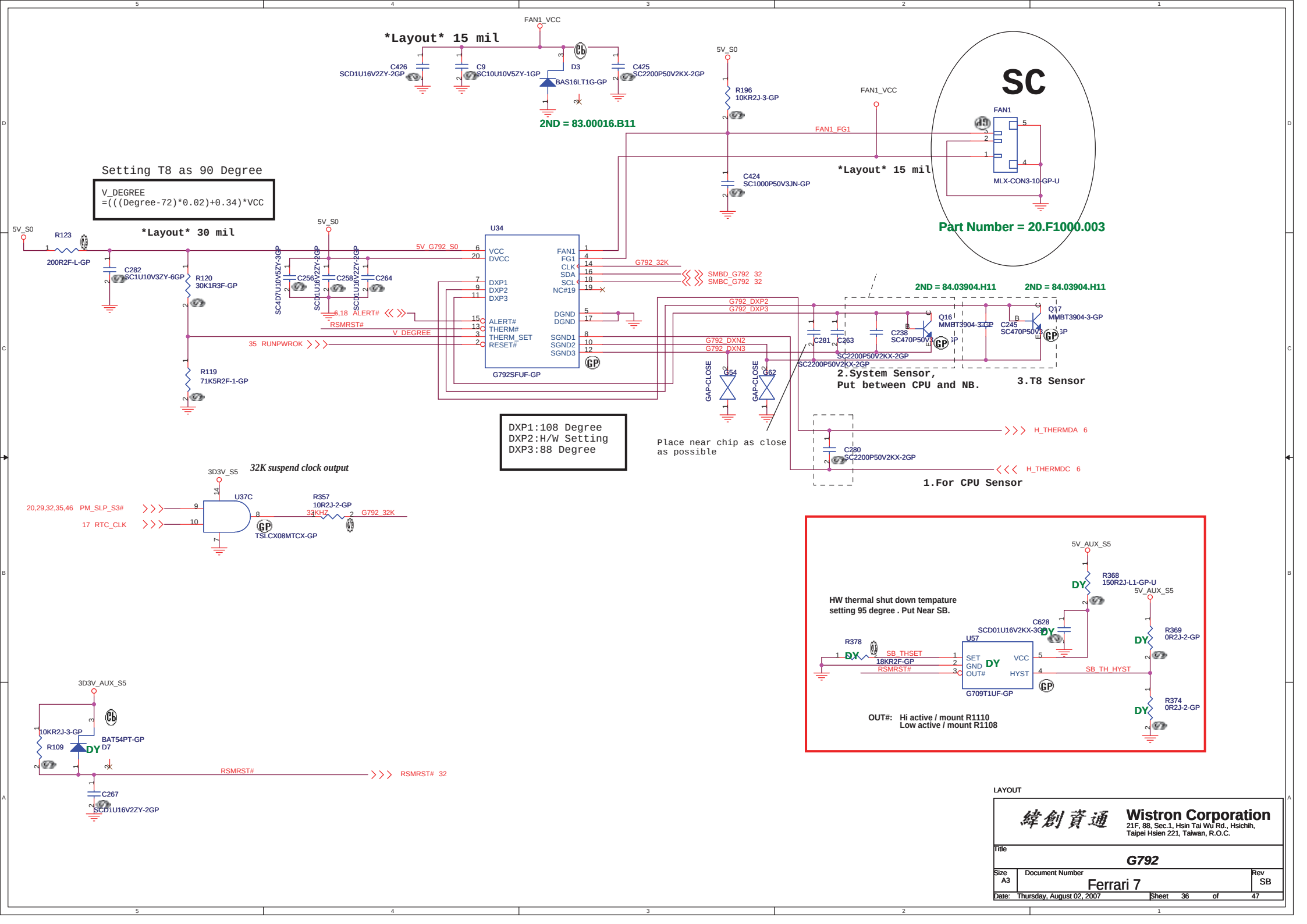


P/H @ 1D8V_S3 PAGE



LAYOUT

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***POWERGOOD&ENABLES(1/2)***	
Size A3	Document Number **Ferrari 7**	Rev SB
Date: Thursday, August 02, 2007	Sheet 35 of 47	


Layout 15 mil
FAN1_VCC
C426
SCD1U16V2ZY-2GP
C9
SC10U10V5ZY-1GP
D3
BAS16LT1G-GP
C425
SC2200P50V2KX-2GP
2ND = 83.00016.B11
5V_S0
R196
10KR2J-3-GP
FAN1_VCC
FAN1_FG1
C424
SC1000P50V3JN-GP
Layout 15 mil
SC
FAN1
MLX-CON3-10-GP-U
Part Number = 20.F1000.003
Setting T8 as 90 Degree
V_DEGREE
=(((Degree-72)*0.02)+0.34)*VCC
Layout 30 mil
5V_S0
R123
200R2F-L-GP
C282
SC1U10V3ZY-6GP
R120
30K1R3F-GP
R119
71K5R2F-1-GP
SC4D7U10V5ZY-3GP
C256
SCD1U16V2ZY-2GP
C258
SCD1U16V2ZY-2GP
C264
5V_S0
5V_G792_S0
U34
VCC
DVCC
DXP1
DXP2
DXP3
ALERT#
THERM#
THERM_SET
RESET#
FAN1
FG1
CLK
SDA
SCL
NC#19
DGND
DGND
SGND1
SGND2
SGND3
G792SFUF-GP
G792_32K
SMBD_G792 32
SMBC_G792 32
6,18 ALERT#
RSMRST#
V_DEGREE
35 RUNPWROK
2ND = 84.03904.H11
2ND = 84.03904.H11
G792_DXP2
G792_DXP3
G792_DXN2
G792_DXN3
Q16
MMBT3904-3-GP
Q17
MMBT3904-3-GP
C281
C263
C238
SC470P50V3
C245
SC470P50V3
SC2200P50V2KX-2GP
SC2200P50V2KX-2GP
GAP-CLOSE
G54
GAP-CLOSE
G62
2.System Sensor,
Put between CPU and NB.
3.T8 Sensor
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
Place near chip as close
as possible
H_THERMDA 6
C280
SC2200P50V2KX-2GP
H_THERMDC 6
1.For CPU Sensor
32K suspend clock output
3D3V_S5
U37C
20,29,32,35,46 PM_SLP_S3#
17 RTC_CLK
R357
10R2J-2-GP
32KHZ
G792_32K
TSLCX08MTCX-GP
HW thermal shut down tempature
setting 95 degree . Put Near SB.
5V_AUX_S5
R368
150R2J-L1-GP-U
5V_AUX_S5
C628
SCD01U16V2KX-3GP
U57
R378
SB_THSET
18KR2F-GP
RSMRST#
SET
GND
OUT#
VCC
HYST
G709T1UF-GP
SB_TH_HYST
R369
0R2J-2-GP
R374
0R2J-2-GP
OUT#: Hi active / mount R1110
Low active / mount R1108
3D3V_AUX_S5
10KR2J-3-GP
R109
BAT54PT-GP
D7
RSMRST#
RSMRST# 32
C267
SCD1U16V2ZY-2GP
LAYOUT
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
G792
Size
A3
Document Number
Ferrari 7
Rev
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Date: Thursday, August 02, 2007
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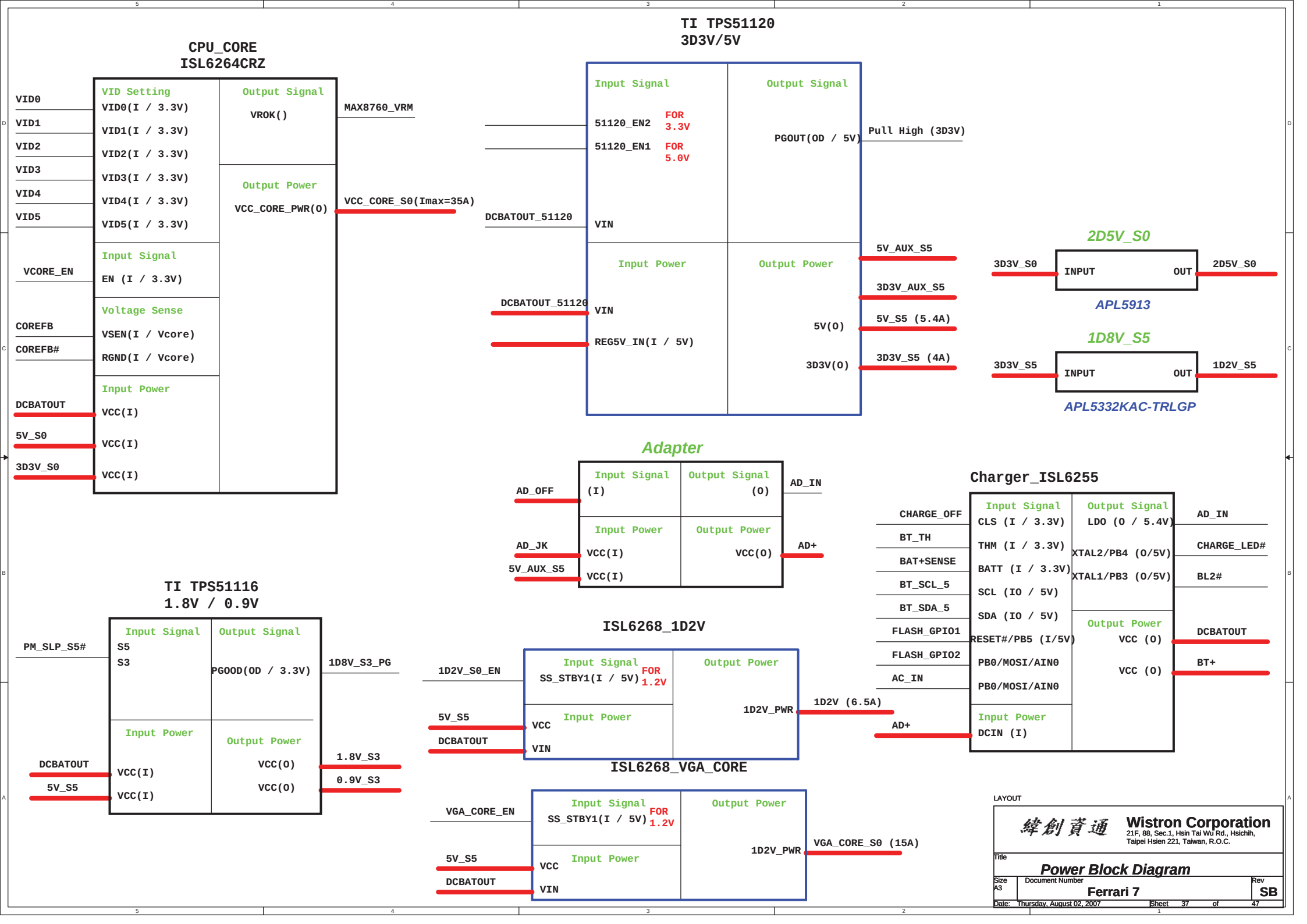
CPU_CORE
ISL6264CRZ
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
Output Signal
VROK()
Output Power
VCC_CORE_PWR(O)
Input Signal
EN (I / 3.3V)
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
Input Power
VCC(I)
VCC(I)
VCC(I)
VID0
VID1
VID2
VID3
VID4
VID5
VCORE_EN
COREFB
COREFB#
DCBATOUT
5V_S0
3D3V_S0
MAX8760_VRM
VCC_CORE_S0(Imax=35A)
TI TPS51120
3D3V/5V
Input Signal
51120_EN2
FOR 3.3V
51120_EN1
FOR 5.0V
VIN
Output Signal
PGOUT(OD / 5V)
Input Power
VIN
REG5V_IN(I / 5V)
Output Power
5V(O)
3D3V(O)
DCBATOUT_51120
DCBATOUT_51120
Pull High (3D3V)
5V_AUX_S5
3D3V_AUX_S5
5V_S5 (5.4A)
3D3V_S5 (4A)
2D5V_S0
3D3V_S0
INPUT
OUT
2D5V_S0
APL5913
1D8V_S5
3D3V_S5
INPUT
OUT
1D2V_S5
APL5332KAC-TRLGP
Adapter
Input Signal
(I)
Output Signal
(O)
Input Power
VCC(I)
VCC(I)
Output Power
VCC(O)
AD_OFF
AD_JK
5V_AUX_S5
AD_IN
AD+
Charger_ISL6255
Input Signal
CLS (I / 3.3V)
THM (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
RESET#/PB5 (I/5V)
PB0/MOSI/AIN0
PB0/MOSI/AIN0
Output Signal
LDO (O / 5.4V)
XTAL2/PB4 (O/5V)
XTAL1/PB3 (O/5V)
Output Power
VCC (O)
VCC (O)
Input Power
DCIN (I)
CHARGE_OFF
BT_TH
BAT+SENSE
BT_SCL_5
BT_SDA_5
FLASH_GPIO1
FLASH_GPIO2
AC_IN
AD+
AD_IN
CHARGE_LED#
BL2#
DCBATOUT
BT+
TI TPS51116
1.8V / 0.9V
Input Signal
S5
S3
Output Signal
PGOOD(OD / 3.3V)
Input Power
VCC(I)
VCC(I)
Output Power
VCC(O)
VCC(O)
PM_SLP_S5#
DCBATOUT
5V_S5
1D8V_S3_PG
1.8V_S3
0.9V_S3
ISL6268_1D2V
Input Signal
SS_STBY1(I / 5V)
FOR 1.2V
Input Power
VCC
VIN
Output Power
1D2V_PWR
1D2V_S0_EN
5V_S5
DCBATOUT
1D2V (6.5A)
ISL6268_VGA_CORE
Input Signal
SS_STBY1(I / 5V)
FOR 1.2V
Input Power
VCC
VIN
Output Power
1D2V_PWR
VGA_CORE_EN
5V_S5
DCBATOUT
VGA_CORE_S0 (15A)
LAYOUT
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Power Block Diagram
Size
A3
Document Number
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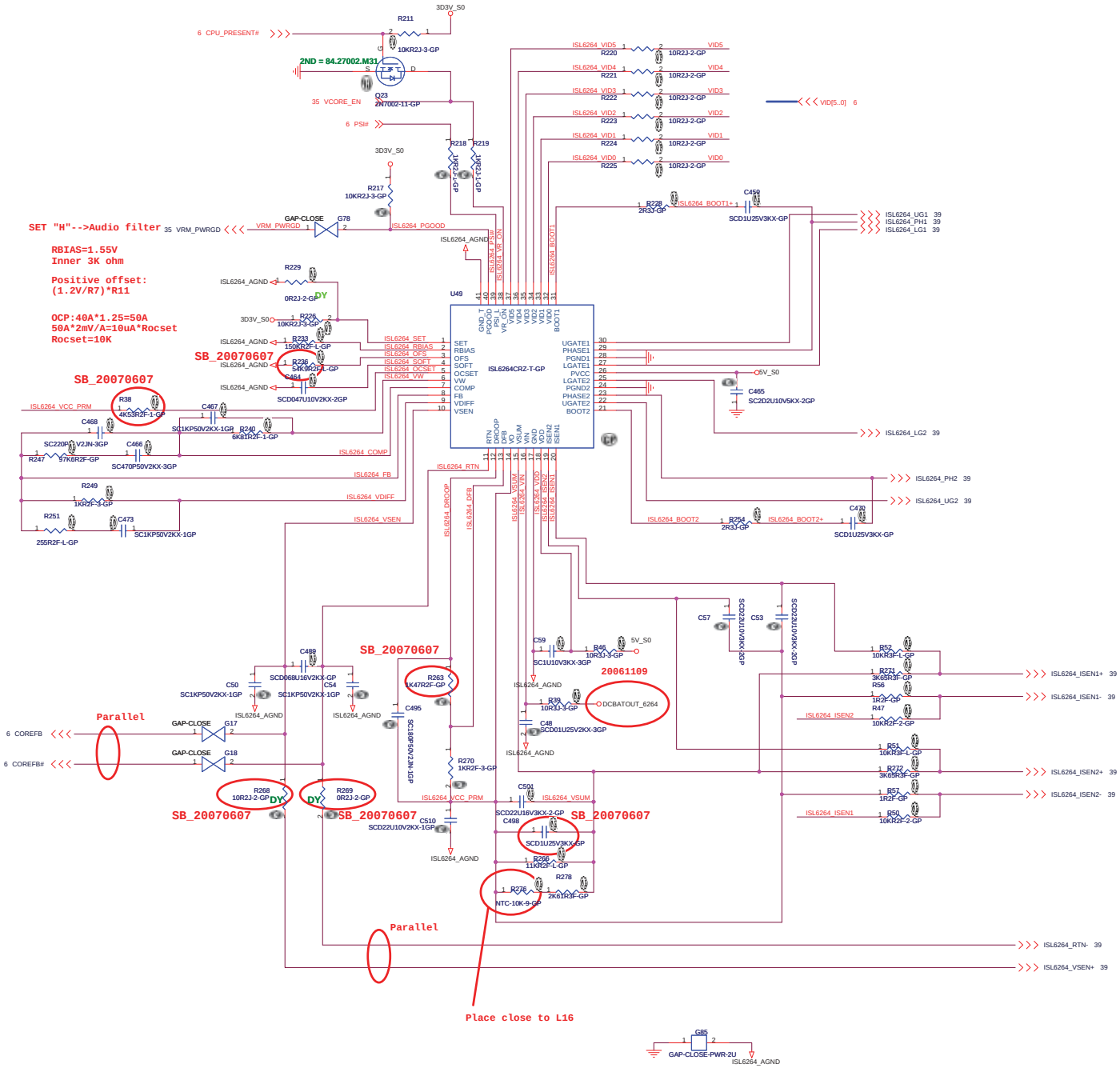
CPU_VCORE
VID=1.075V
Iomax=35A
OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.525
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	0	1	1	1	0.975
0	1	1	0	0	0	0.950
0	1	1	0	0	1	0.925
0	1	1	0	1	0	0.900
0	1	1	0	1	1	0.875
0	1	1	1	0	0	0.850
0	1	1	1	0	1	0.825
0	1	1	1	1	0	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.75
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.725
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7
1	1	1	1	1	1	0.375



LAYOUT

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU Vcore Power_1*

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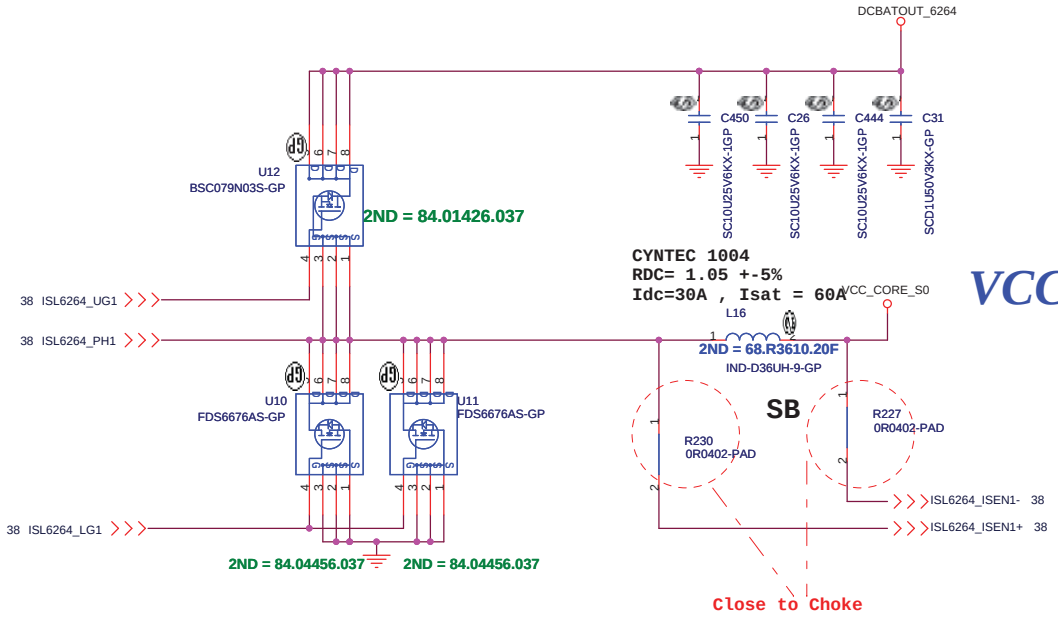
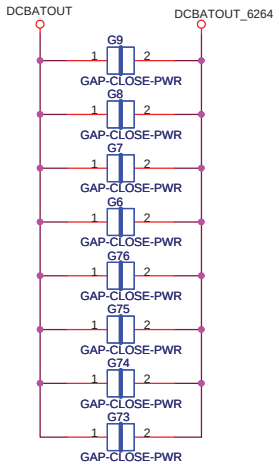
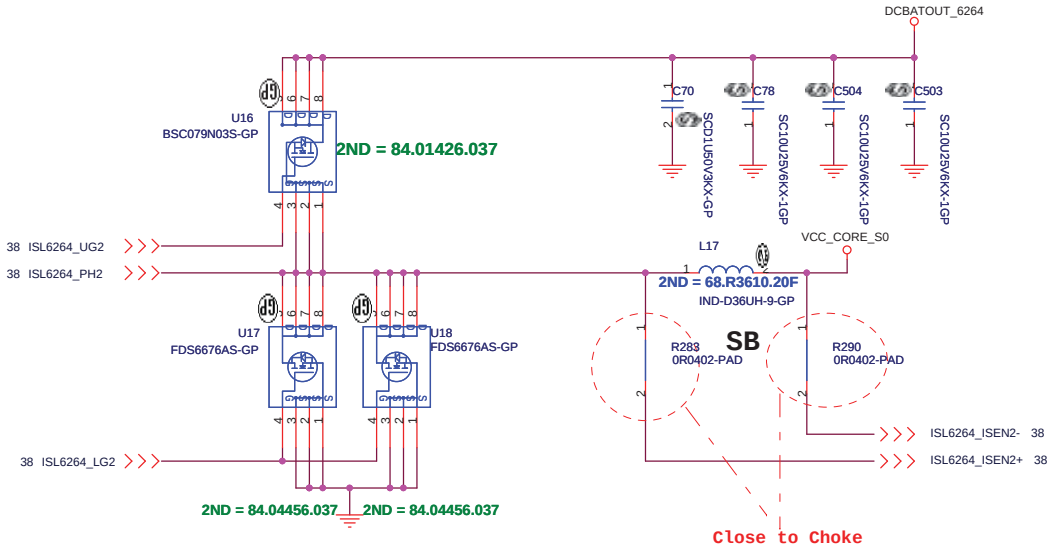
20061109

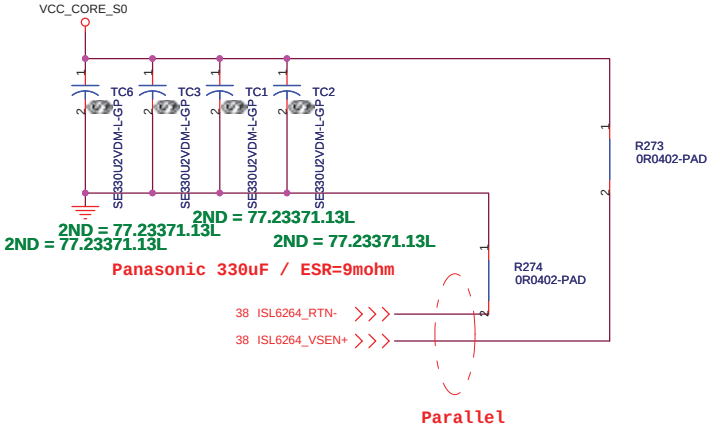


VCC_CORE_S0





CYNTEC 1004
RDC= 1.05 +-5% , Idc=30A , Isat = 60A



LAYOUT

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU Vcore Power_2***	
Size A3	Document Number **Ferrari 7**	Rev SB
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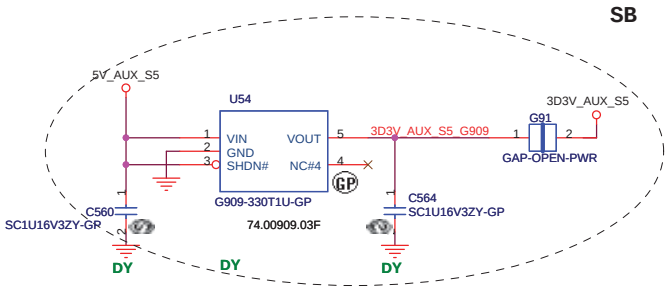
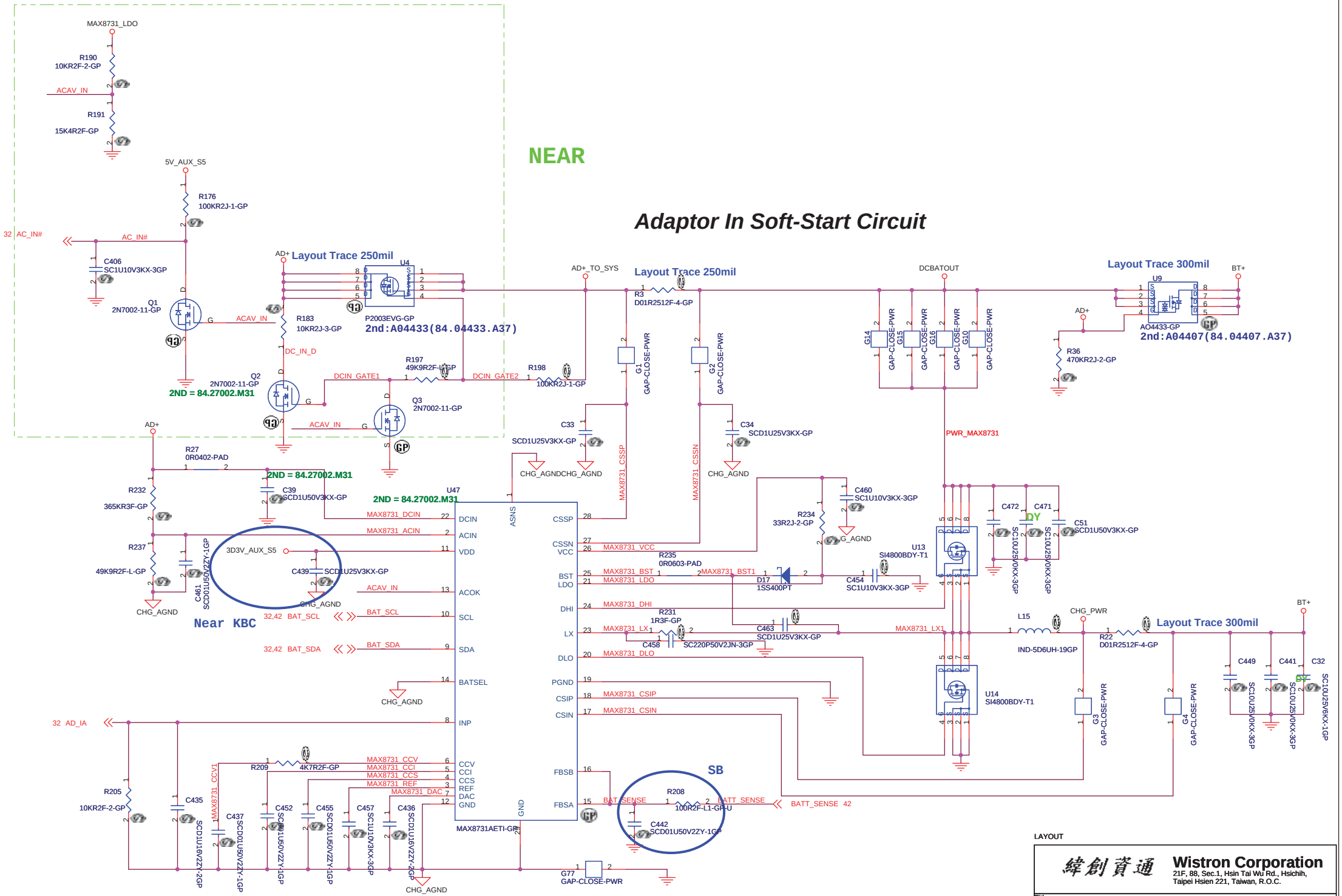
Aux Power 3D3V_AUX_S5



LAYOUT

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***3D3V_AUX***
Size A3	Document Number **Ferrari 7** Rev **SB**
Date: Thursday, August 02, 2007	Sheet 40 of 47



LAYOUT

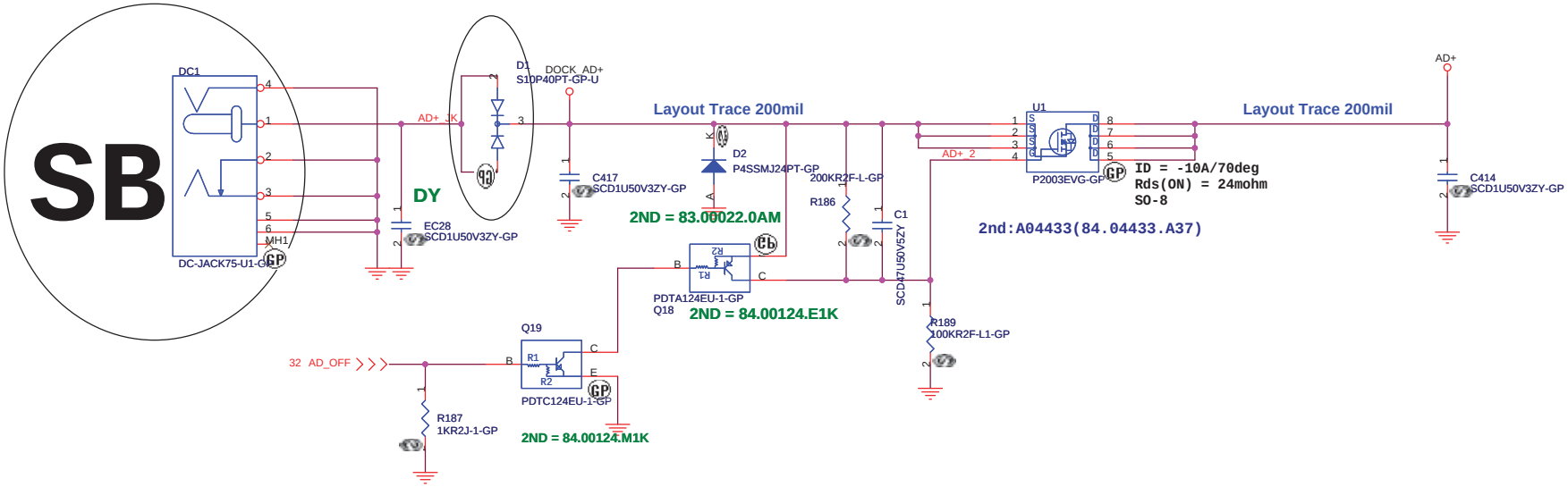
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER MAX8731

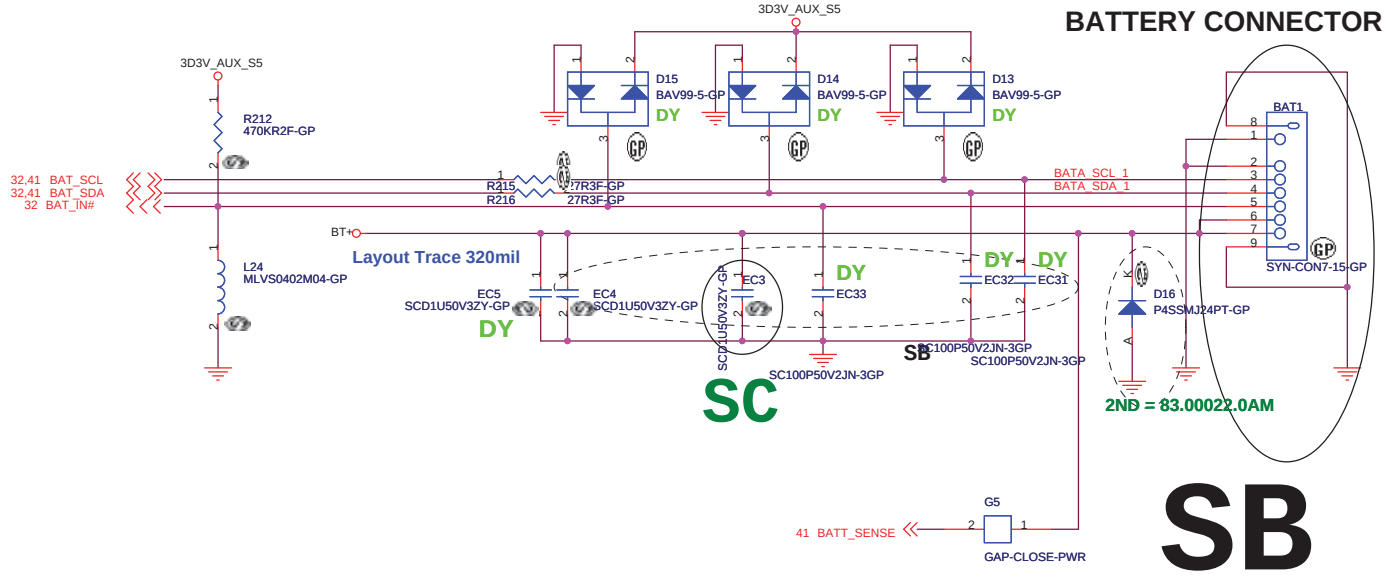
Size: A3 | Document Number: Ferrari 7 | Rev: SD

Date: Thursday, August 02, 2007 | Sheet 41 of 47

Adaptor in to generate DCBATOUT

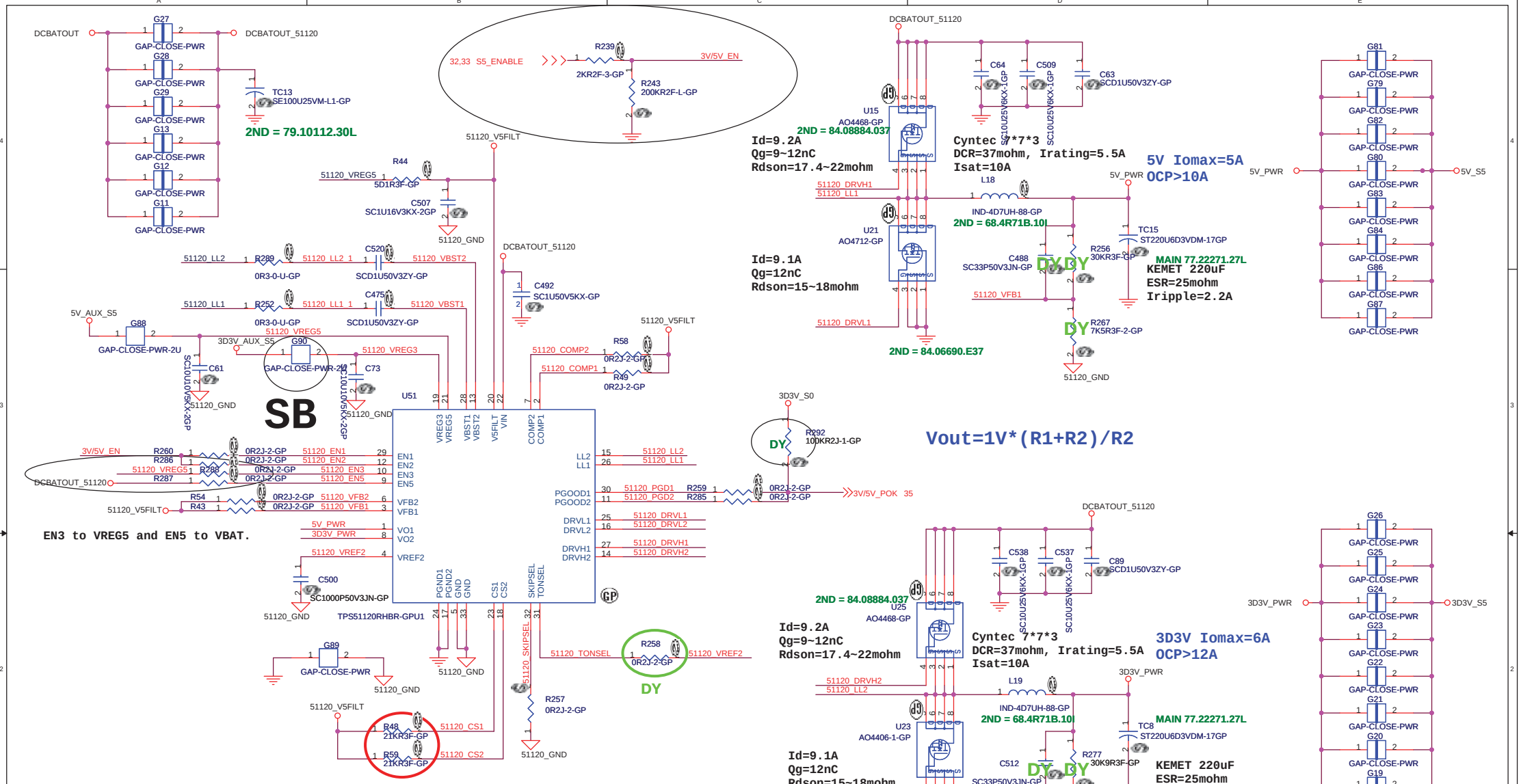


BATTERY CONNECTOR



LAYOUT

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**AD/BATT CONN**
Size A3	Document Number **Ferrari 7** Rev **SB**
Date: Thursday, August 02, 2007	Sheet 42 of 47



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	Switcher OFF	not use	Swither ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

LAYOUT

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51120 5V 3D3V

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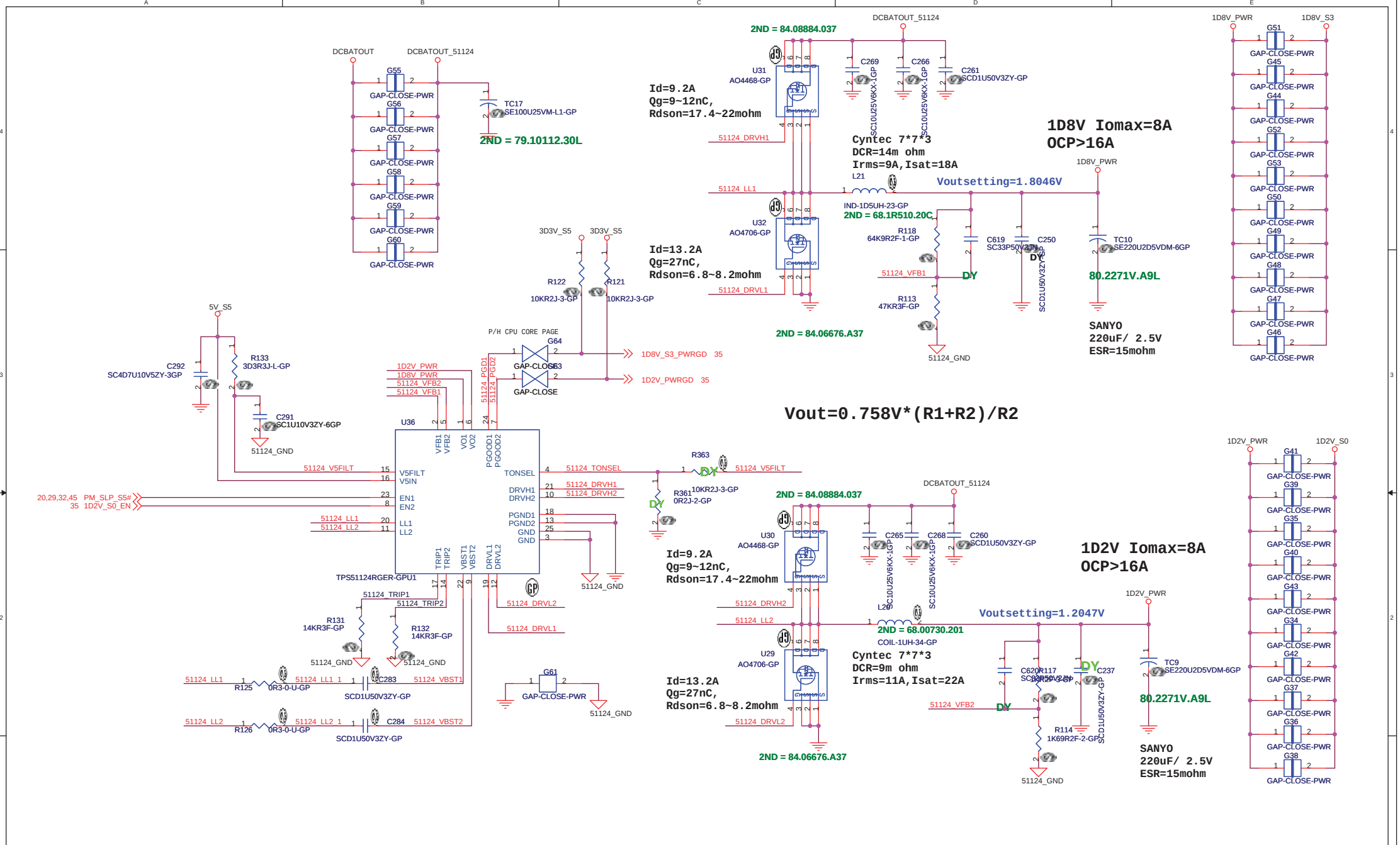

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

LAYOUT

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *TPS51124_1D8V_1D2V*

Size: A3 | Document Number: Ferrari 7 | Rev: SB

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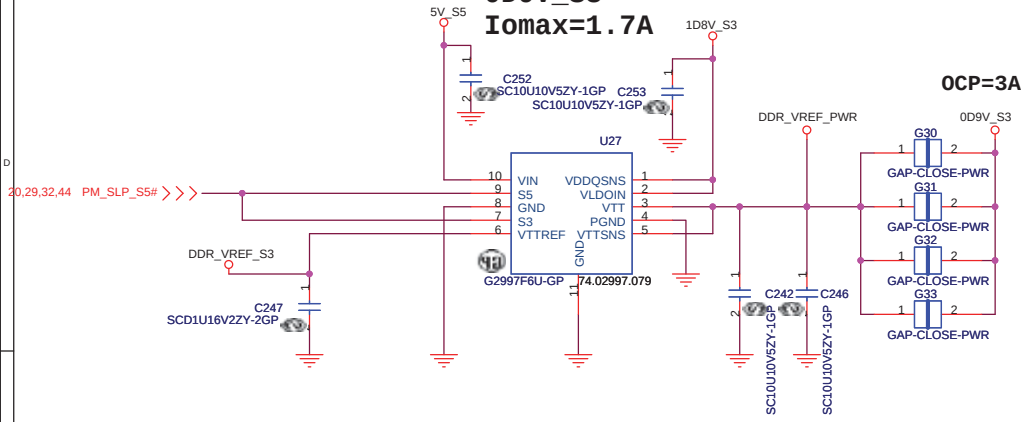
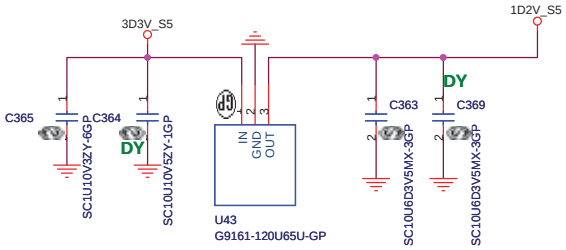
0D9V_S3
Iomax=1.7A



OCP=3A

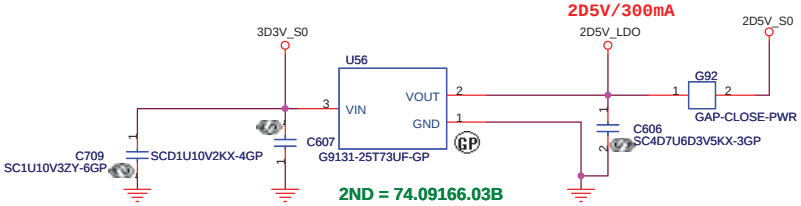
1D2V_S5
Iomax=400mA



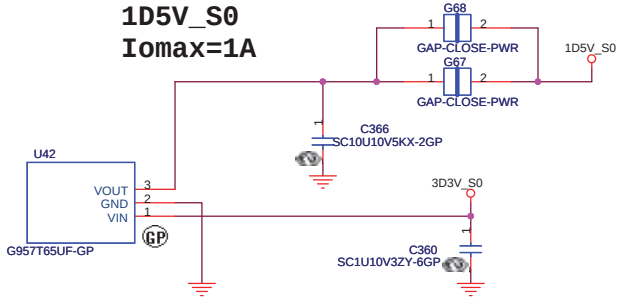
Place near to SB600

G957

2D5V_S0
Iomax=0.3A

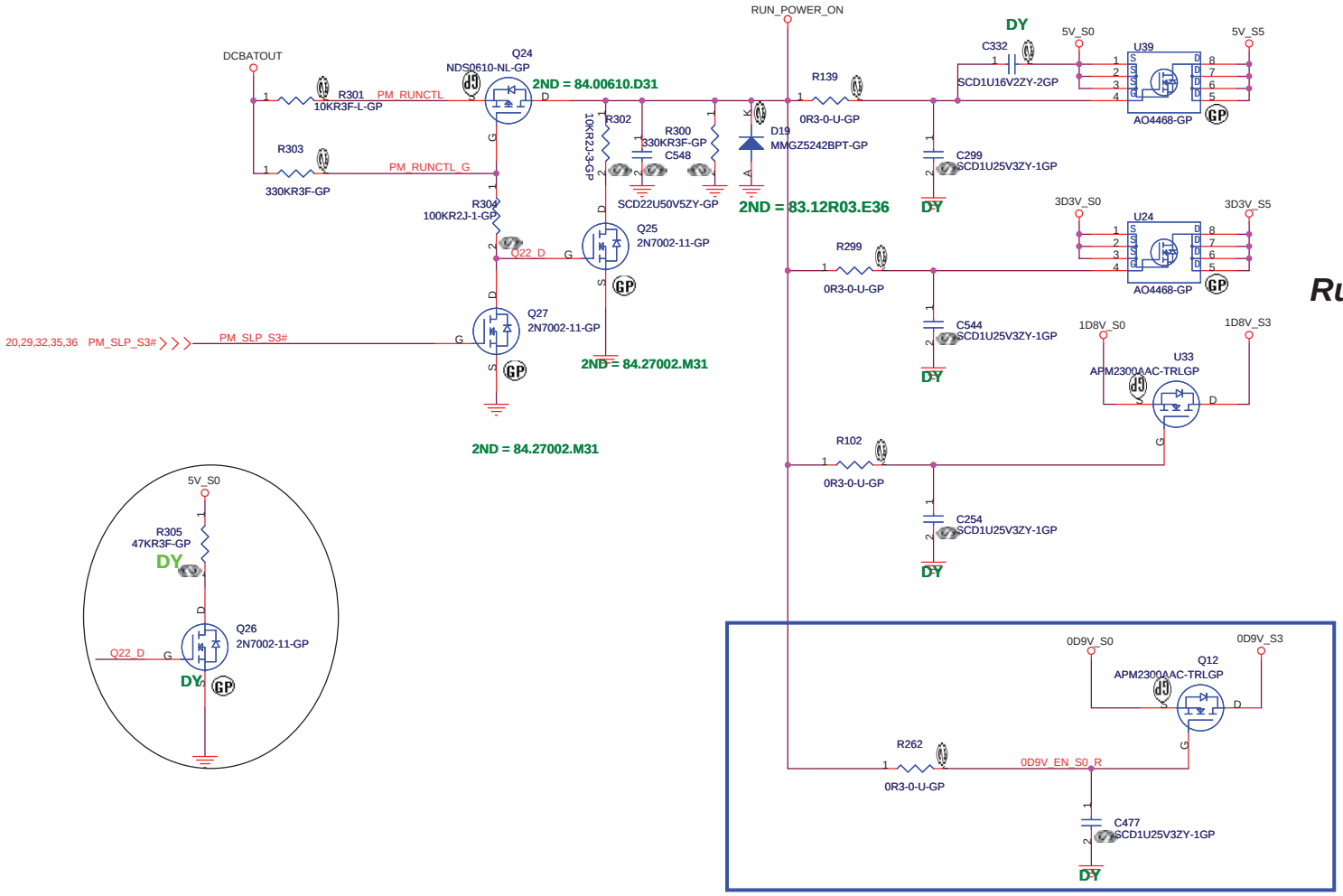


1D5V_S0
Iomax=1A



LAYOUT

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***2D5V/1D5V/0D9V***
Size A3	Document Number **Ferrari 7** Rev **SB**
Date: Thursday, August 02, 2007	Sheet 45 of 47



Run Power

LAYOUT

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PWR CTL LOGIC / PWR PLANE***

Size	Document Number	Rev
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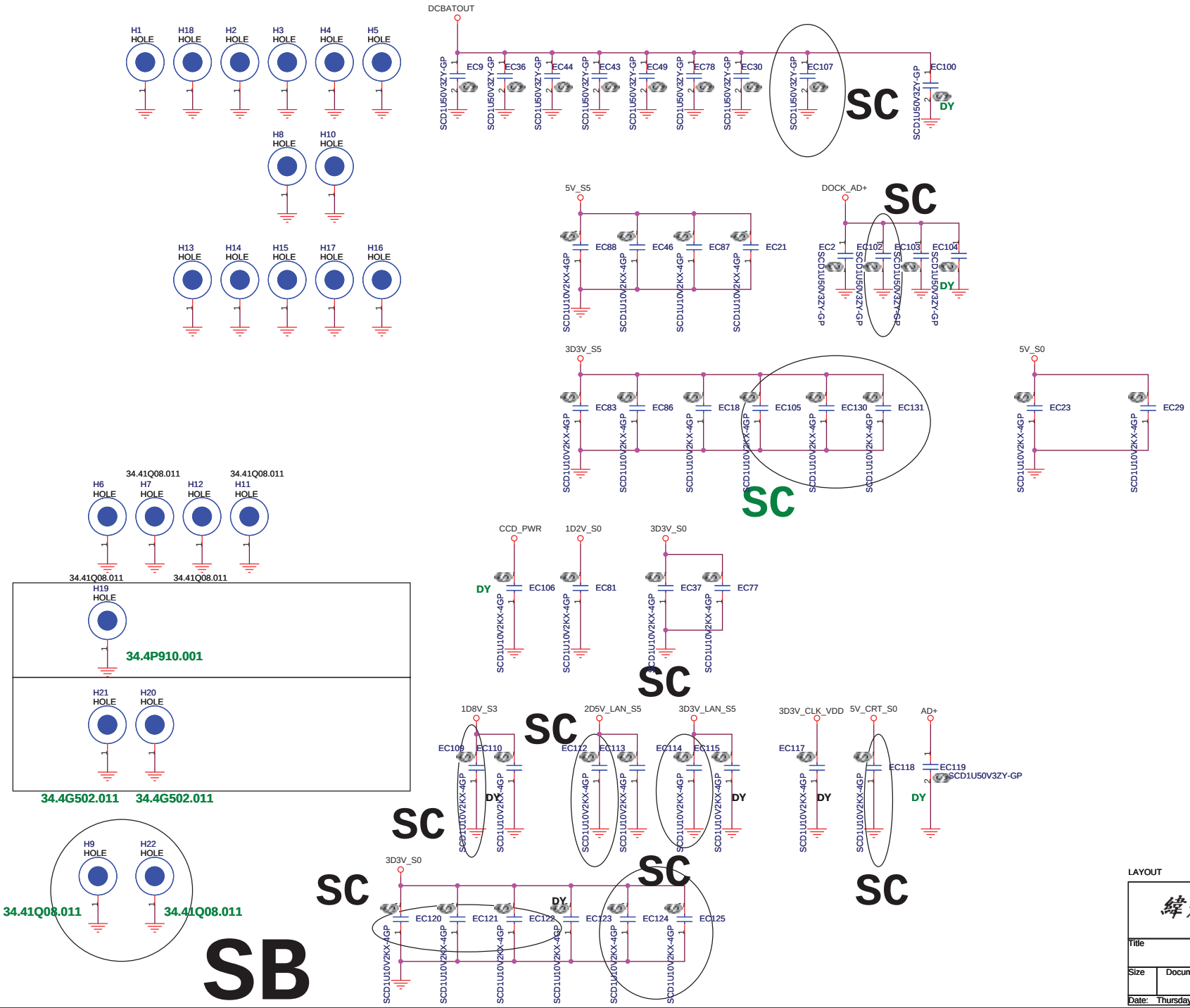

LAYOUT

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI/Spring/Boss***

Size | Document Number: **Ferrari 7** | Rev: SB

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